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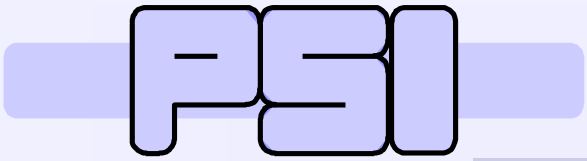
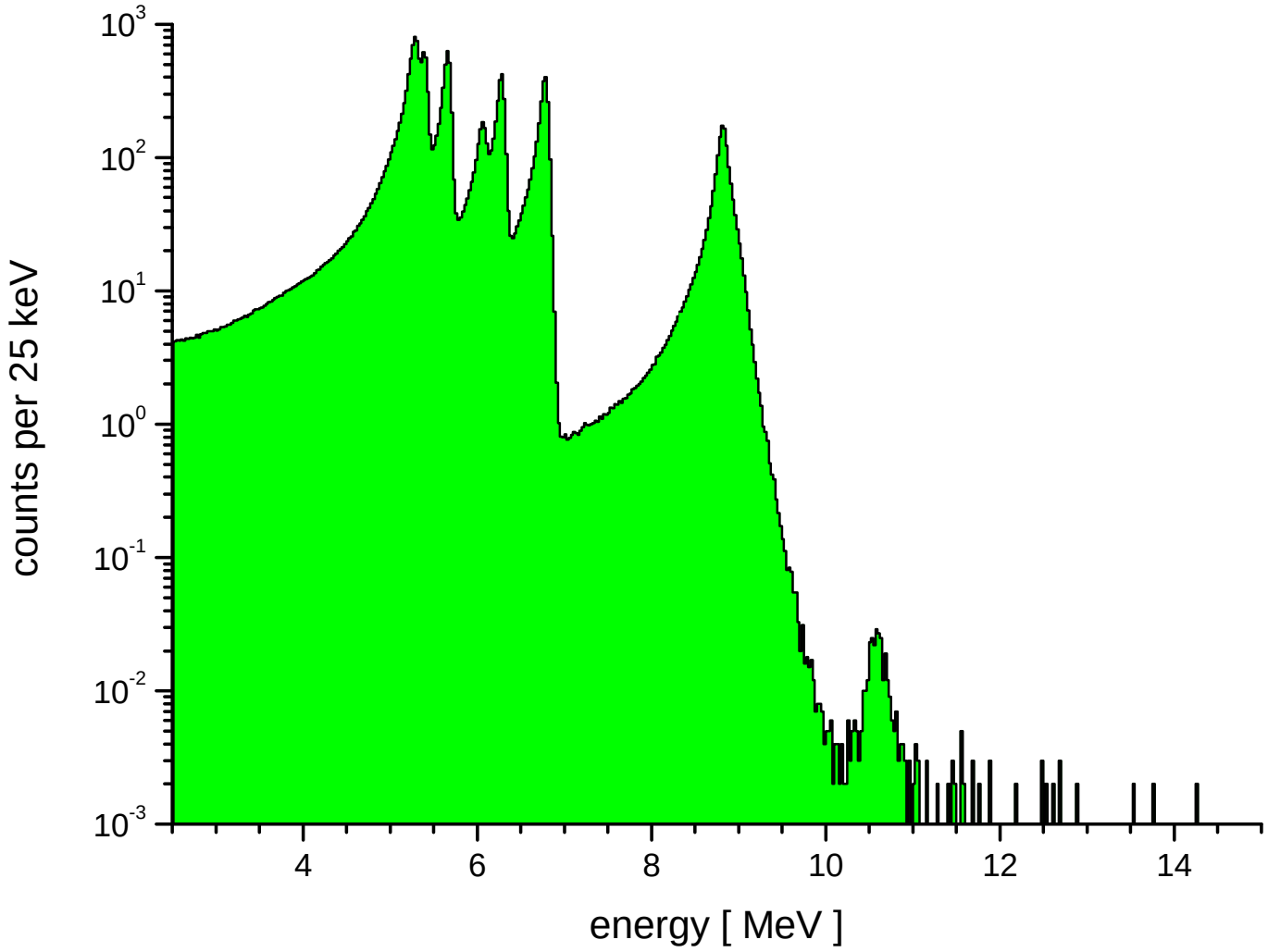


pureCOLD for β-α pile-up suppression a status report

R. Dressler, P. Rasmussen, R. Eichler, N. Schlumpf

First results TAN 07

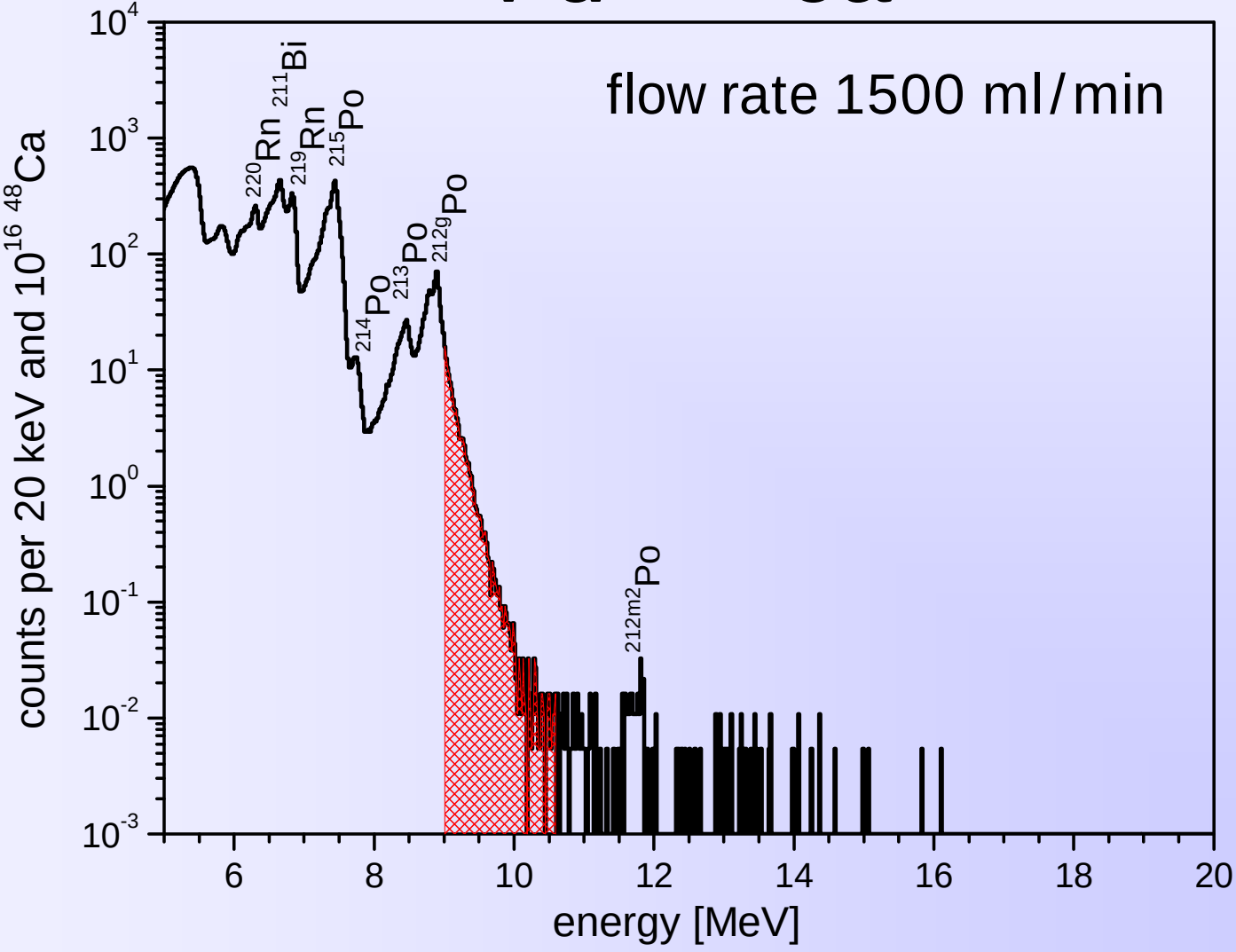


Pile-Up Rejection Electronics for Cryo On-Line Detector **pureCOLD**

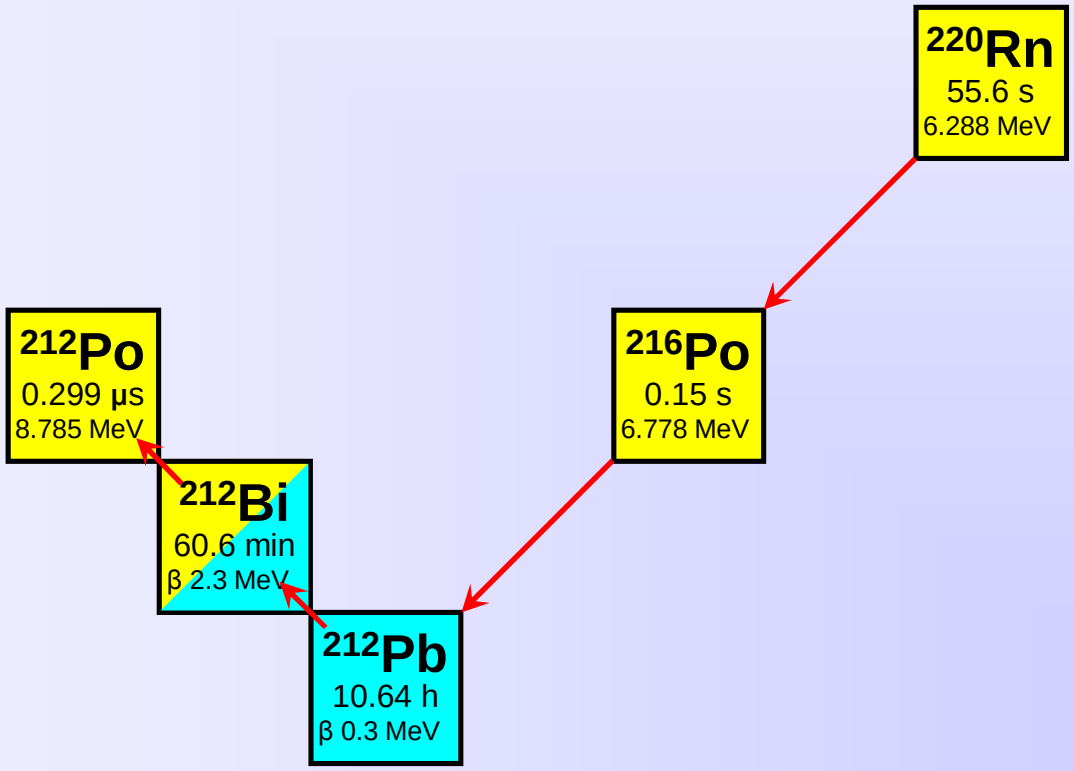
Outline

- Introduction
- Final hardware design
- First measurements
- Outlook

β-α pile-up spectrum
$^{244}Pu + ^{48}Ca$

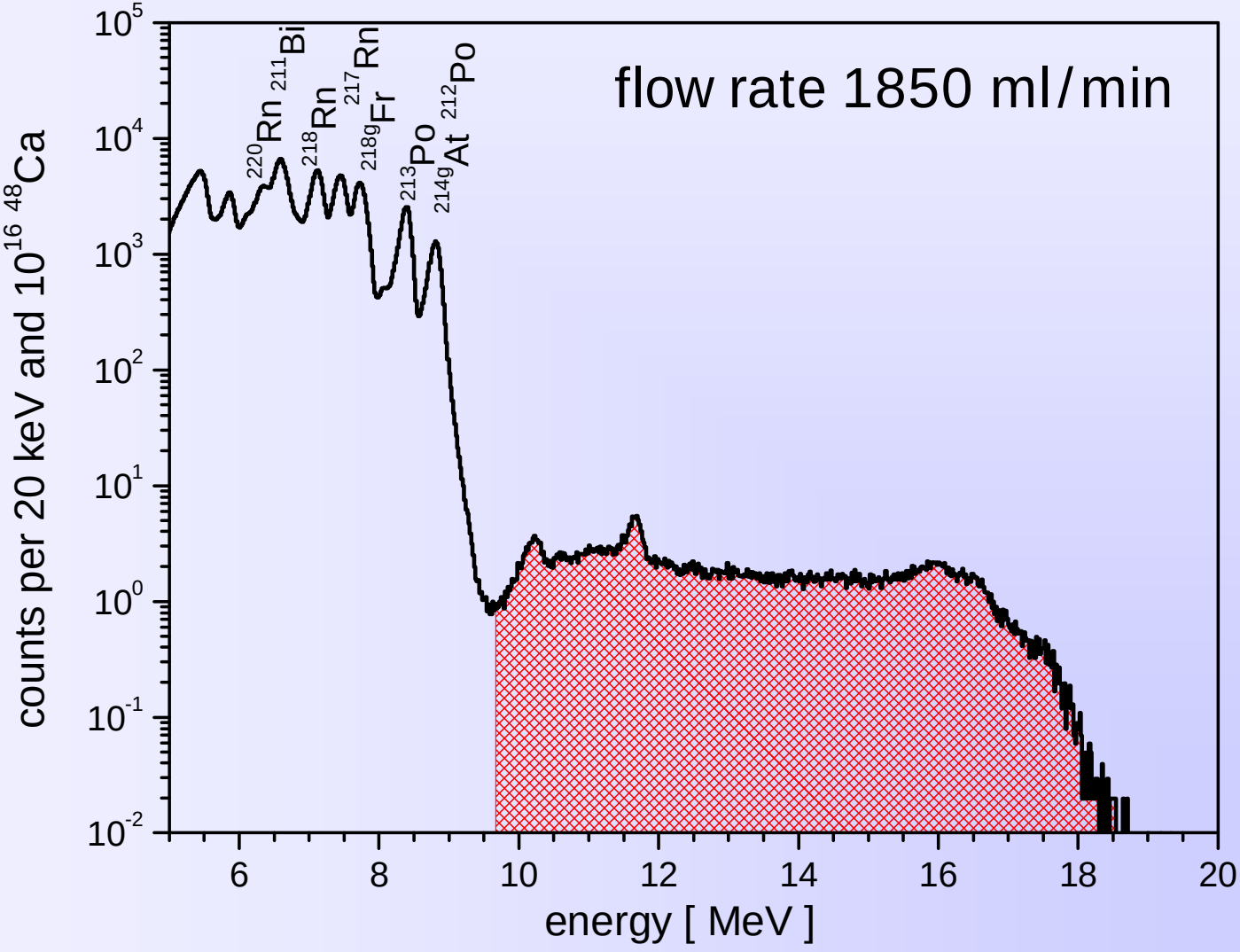


β-α pile-up problem

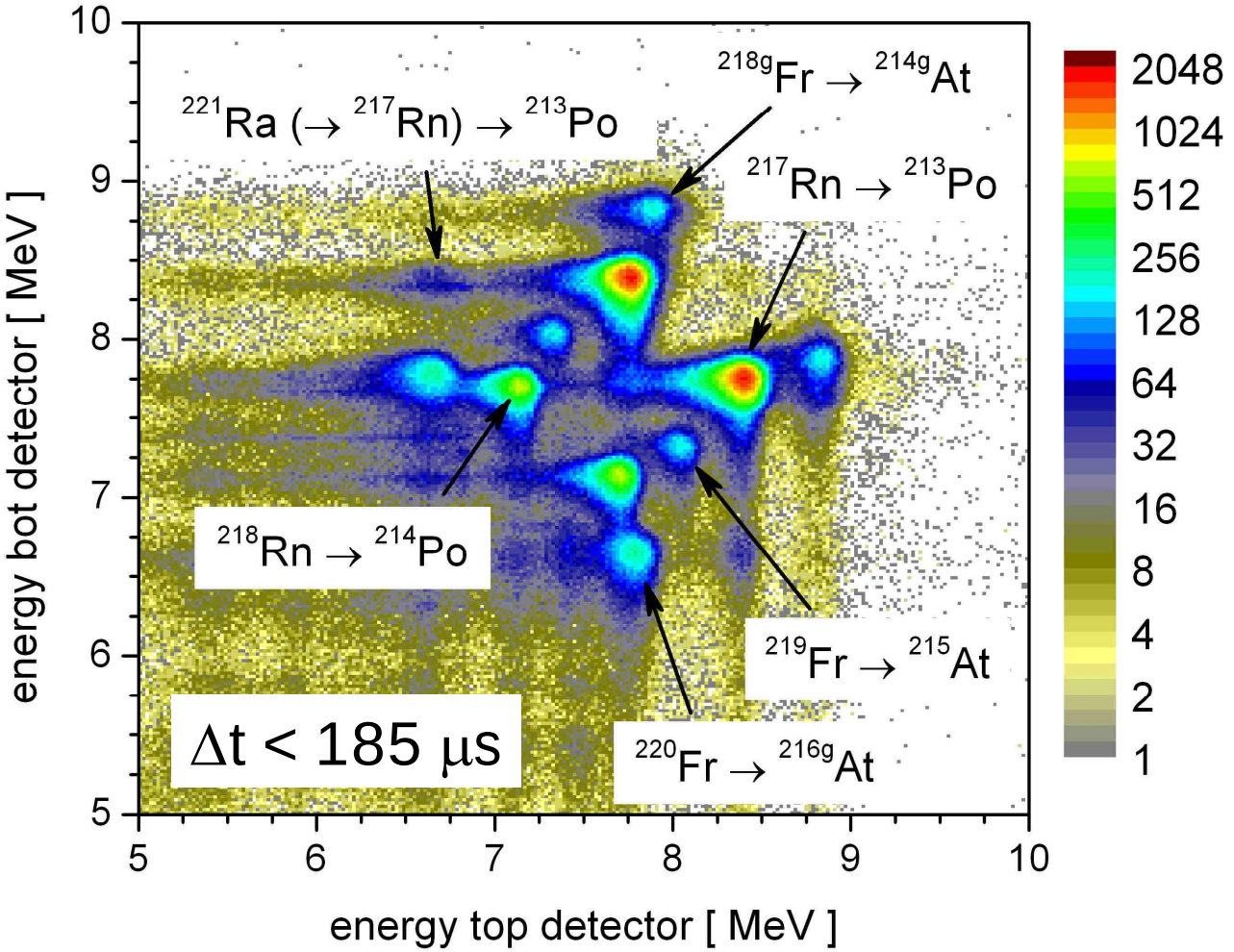


α-α pile-up spectrum

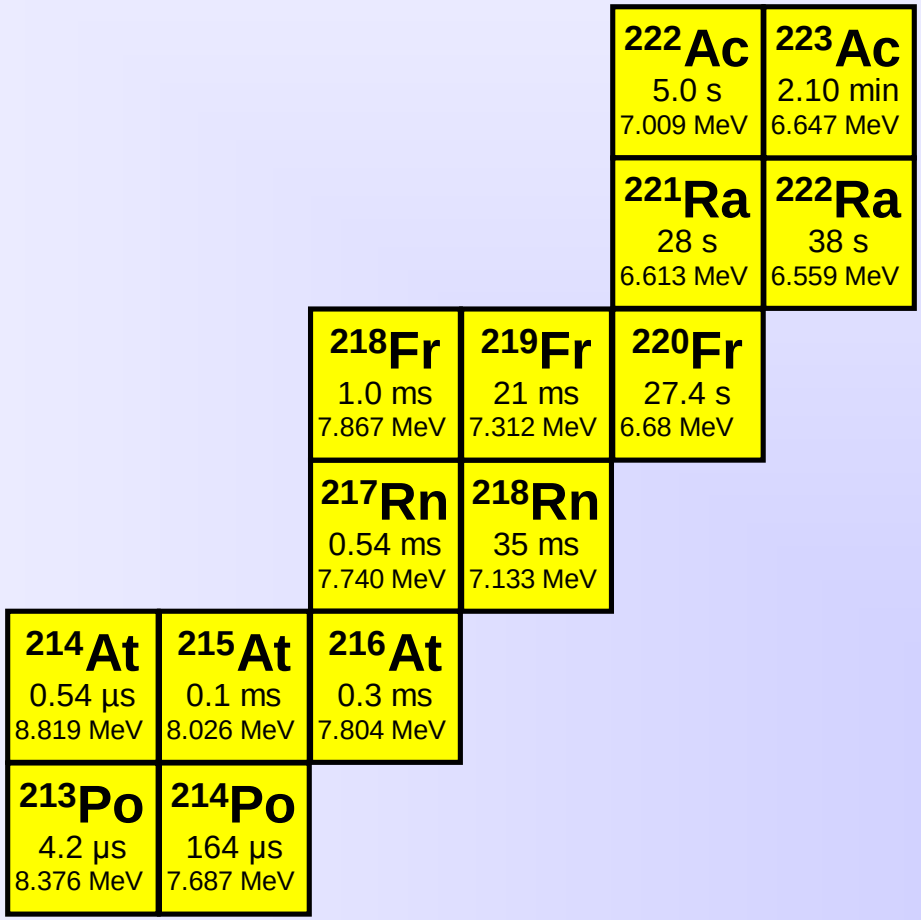
$^{244}Pu + {}^{48}Ca$



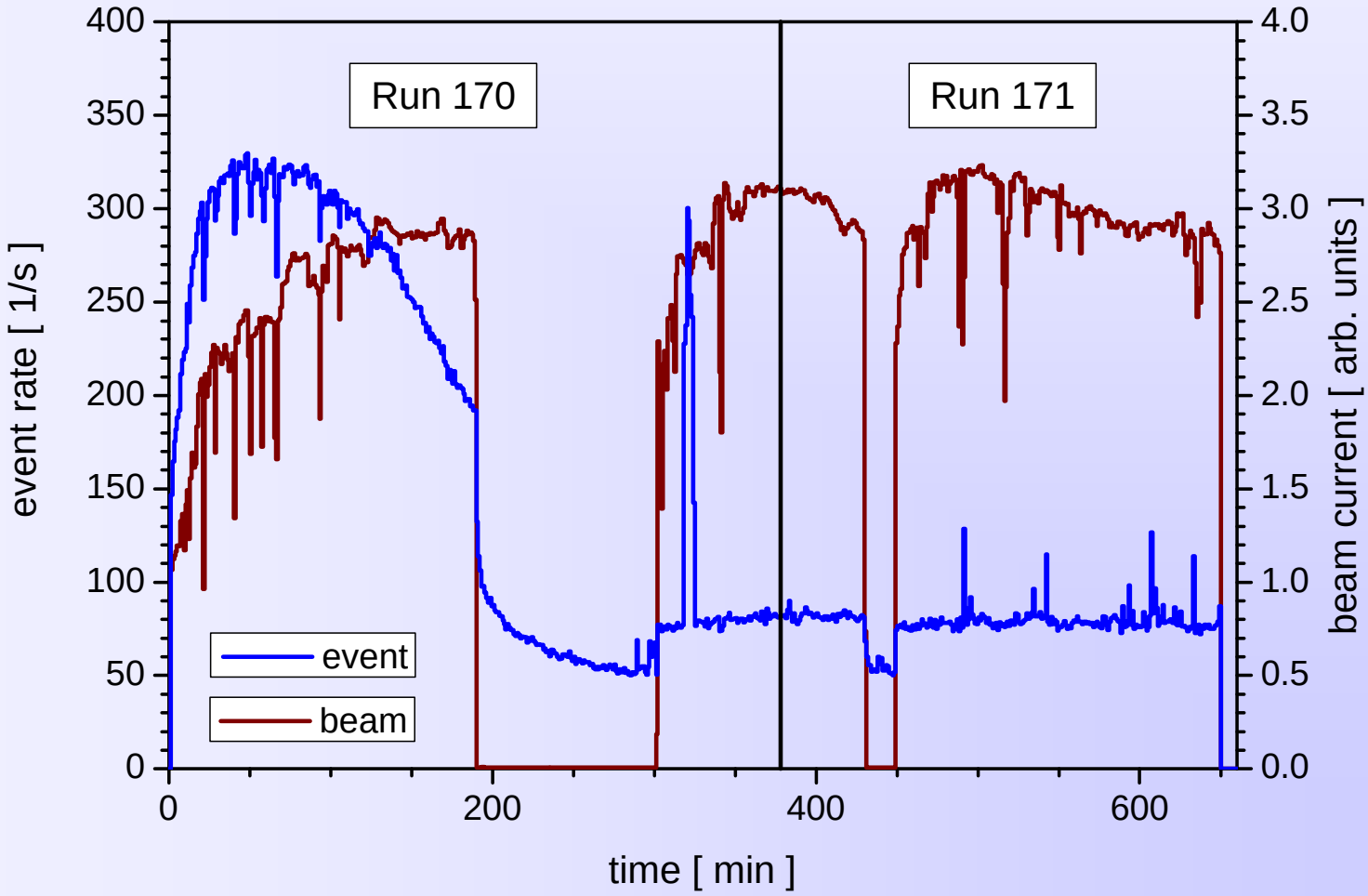
α-α correlations ^{244}Pu + ^{48}Ca



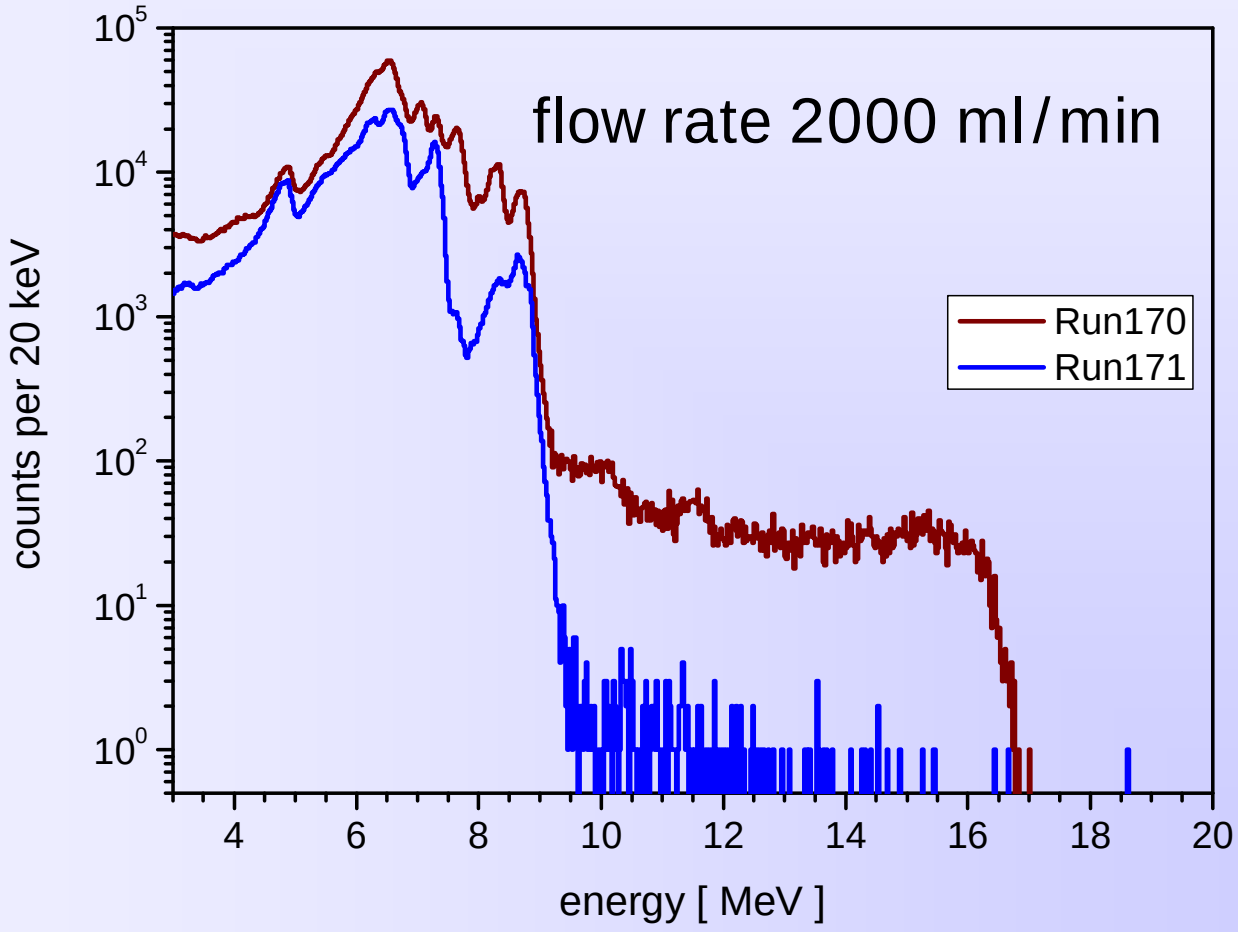
α-α pile-up problem



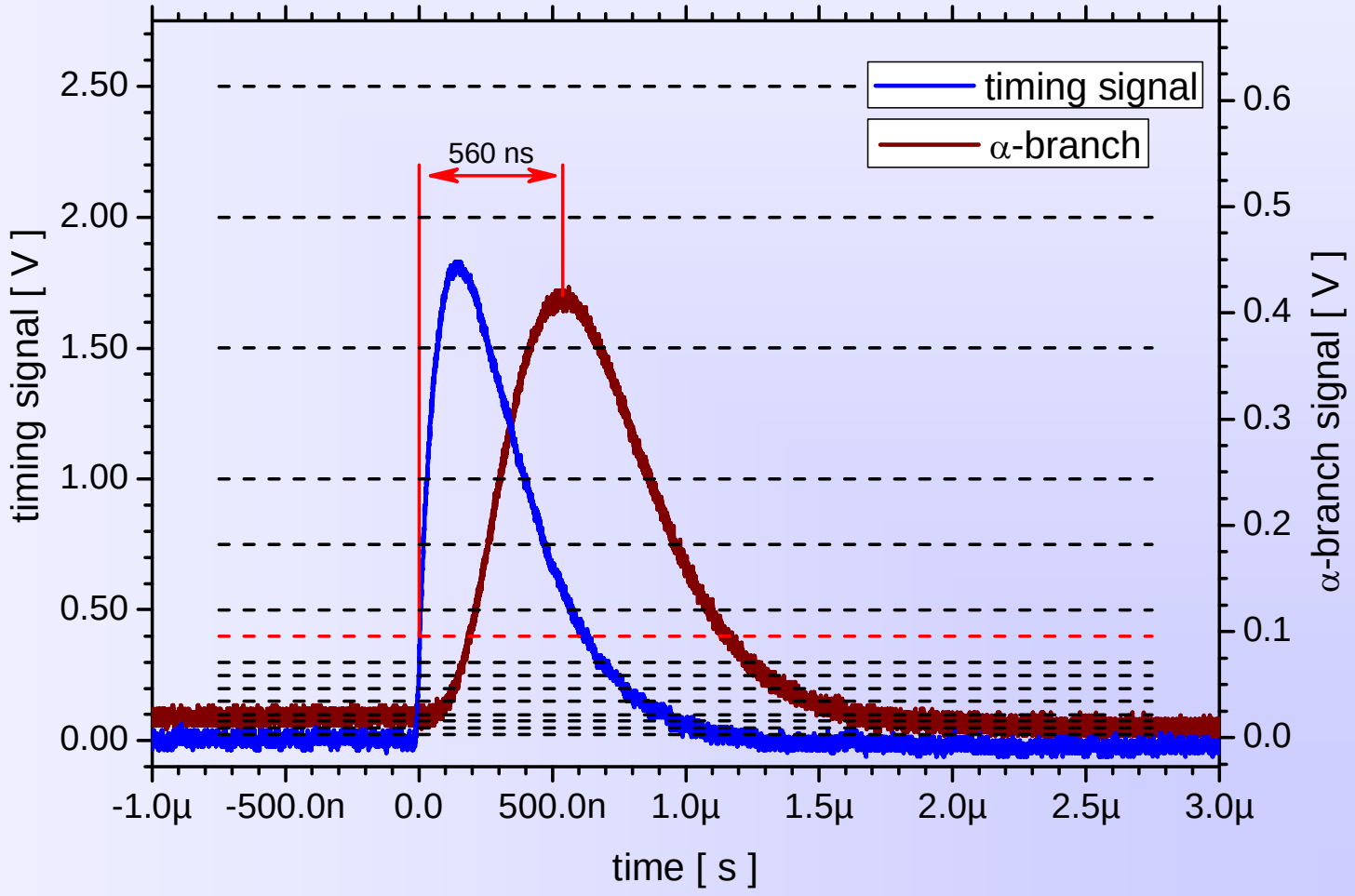
Aerosol formation with H_2O ?



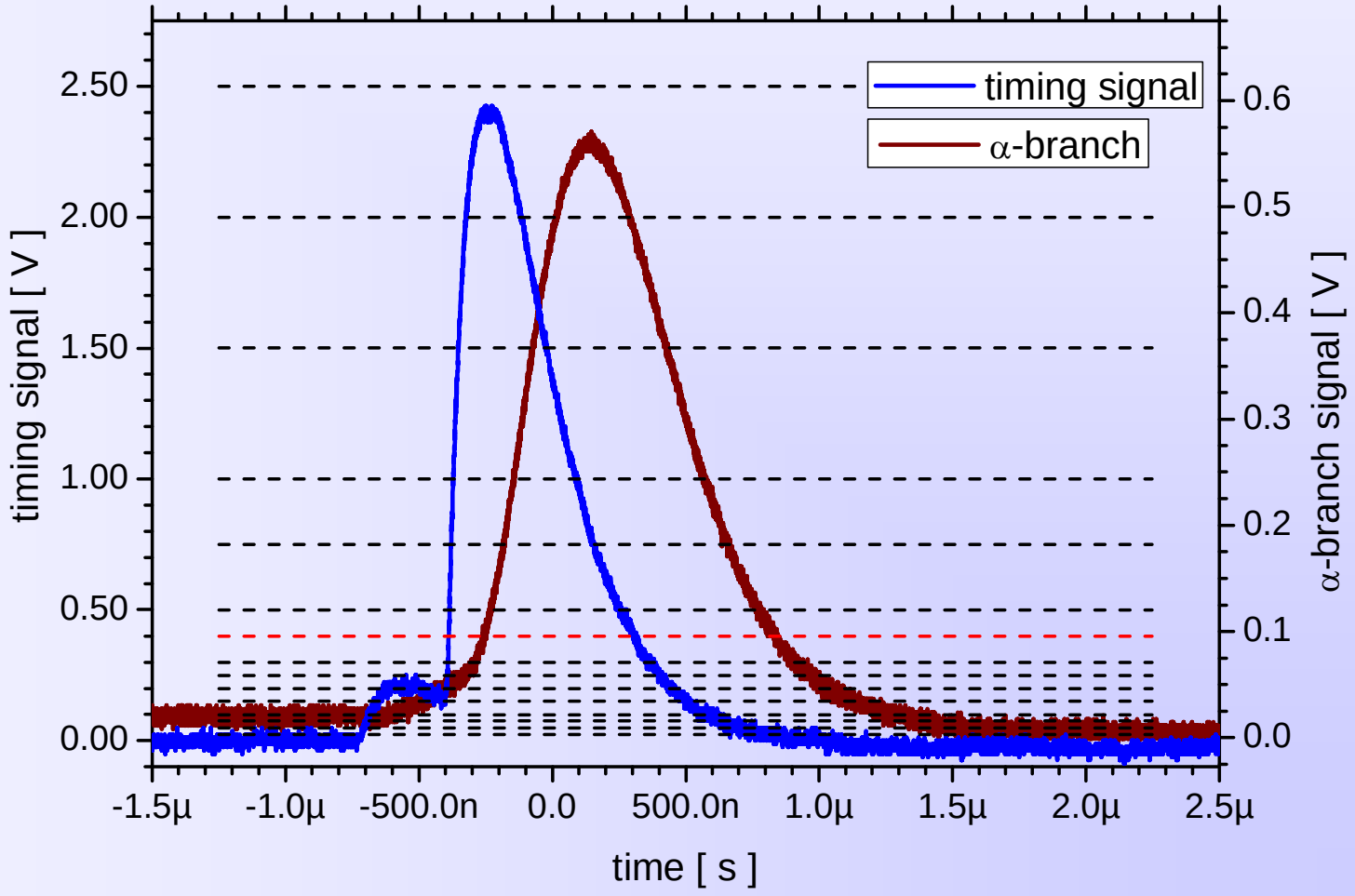
Aerosol formation with H_2O ?



Working principle

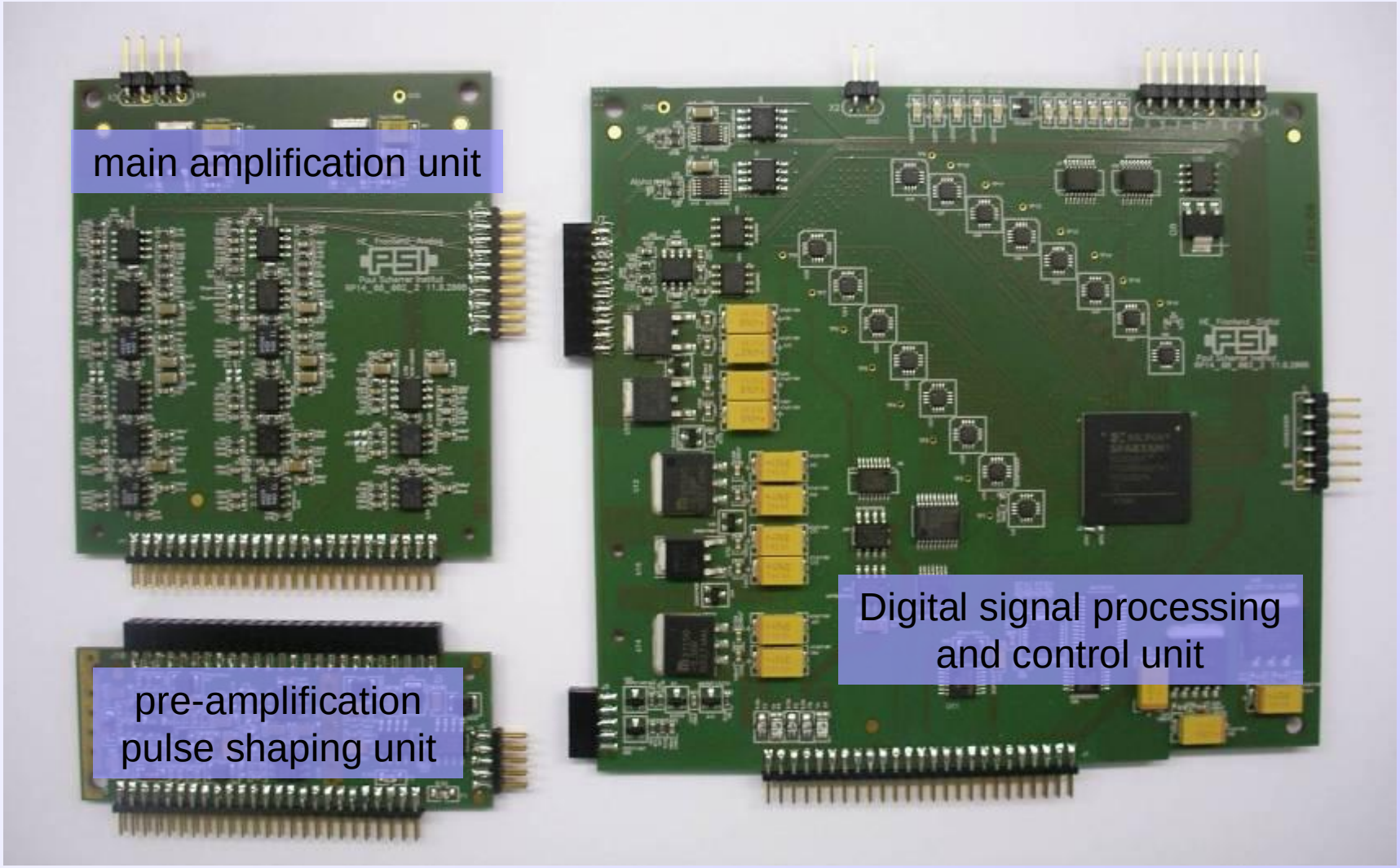


Working principle



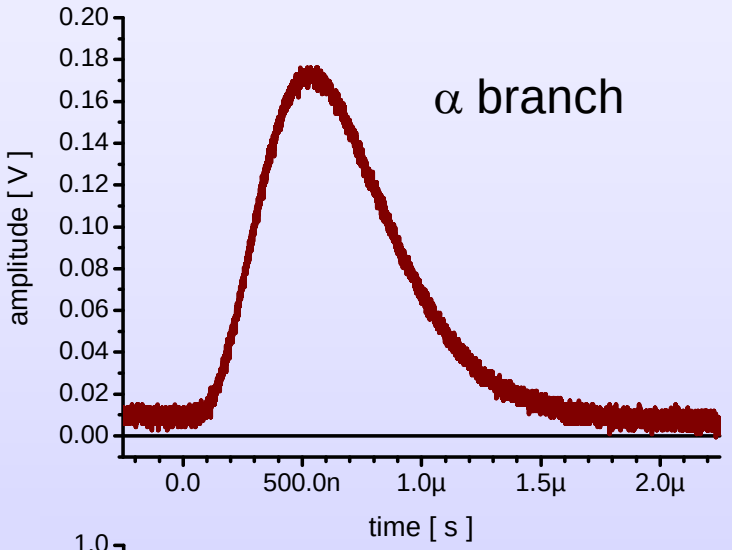
Final hardware design

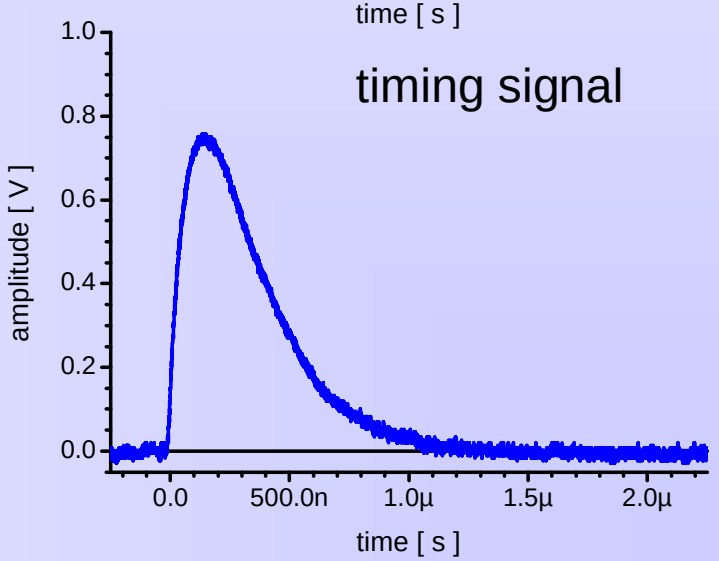
Frontend PCB design



Preamplifier / Shaper / Amplifier

- pre-amplifier
  - *gain 10*
  - *shaping time 220 ns*
- main amplifier
  - *separate α- and SF-branch*
  - *fixed gains*
    α: 7.5MeV, 15MeV, 30MeV
    SF: 75MeV, 150MeV, 300MeV
  - *fast timing amplifier*
  - *fixed gains*
    3MeV, 9MeV, 15MeV
- signal width
  - *375 ns timing signal*
  - *650 ns spectroscopic signal*

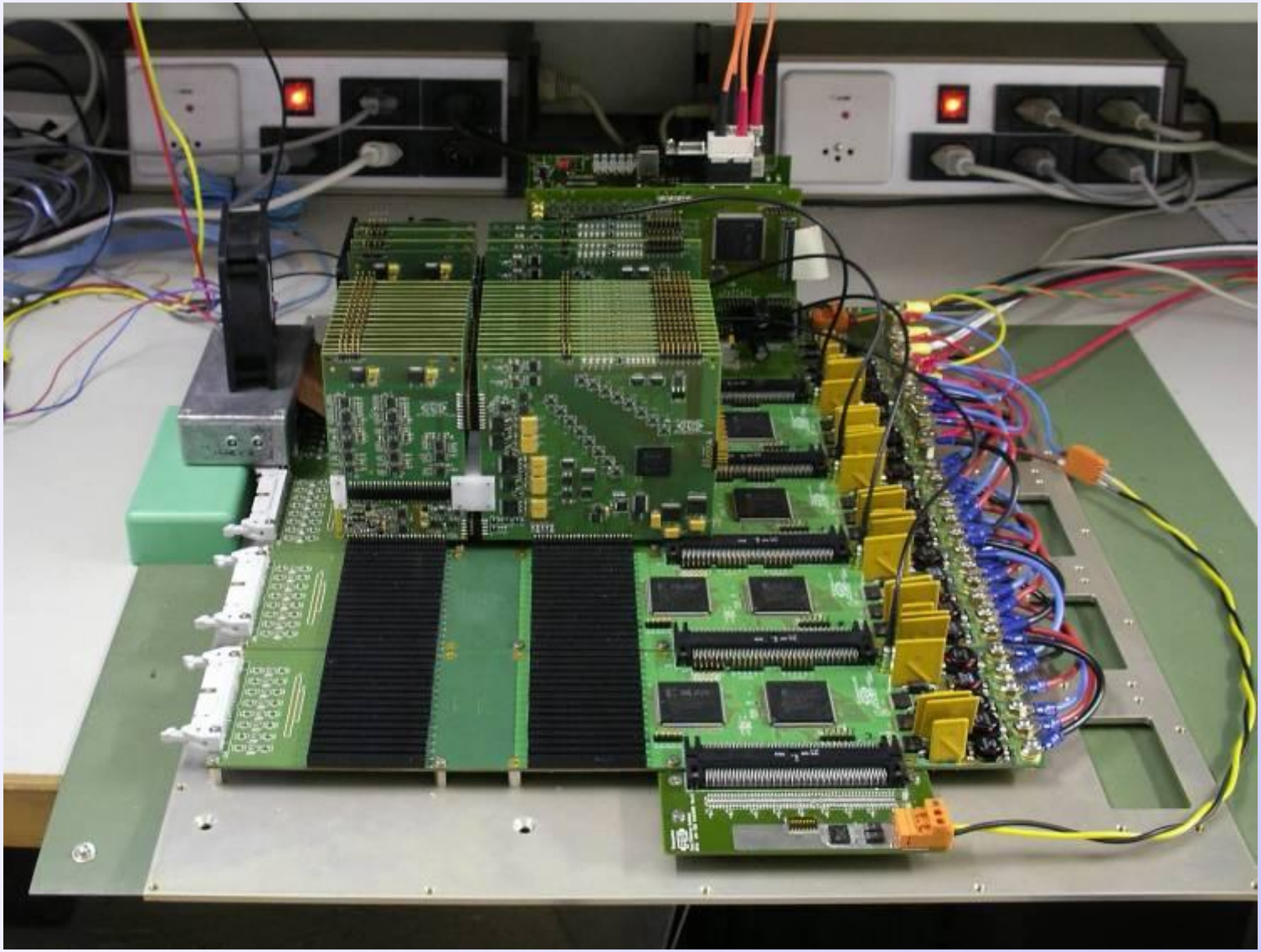




ADC / Comparator / FPGA

- 16 × fast comparators
  - *150 ps delay, 10 ps jitter*
  - *run-time matching via cable delay better 0.7 ps*
  - *levels adjustable via DAC*
- 8 phase clock
  - *4 × 250 MHz DDR clock*
  - *45° phase shift*
  - *run-time matching via cable delay better 0.3 ps*
  - *time resolution 0.5 ns*
- 2 × ADC
  - *500 kSamples/s*
  - *16 bit conversion depth*
  - *2.5 V bipolar range*
  - *120 ns conversion time*
  - *1.8 µs serial read-out time*
- Spartan 3 FPGA
  - *340 event FIFO*
  - *110 µs serial transfer to MB*
  - *max. rate 9 kevents per sec*
  - *time between consecutive events 4 µs*
  - *7x free programmable interconnection signals*

Main-board PCB design



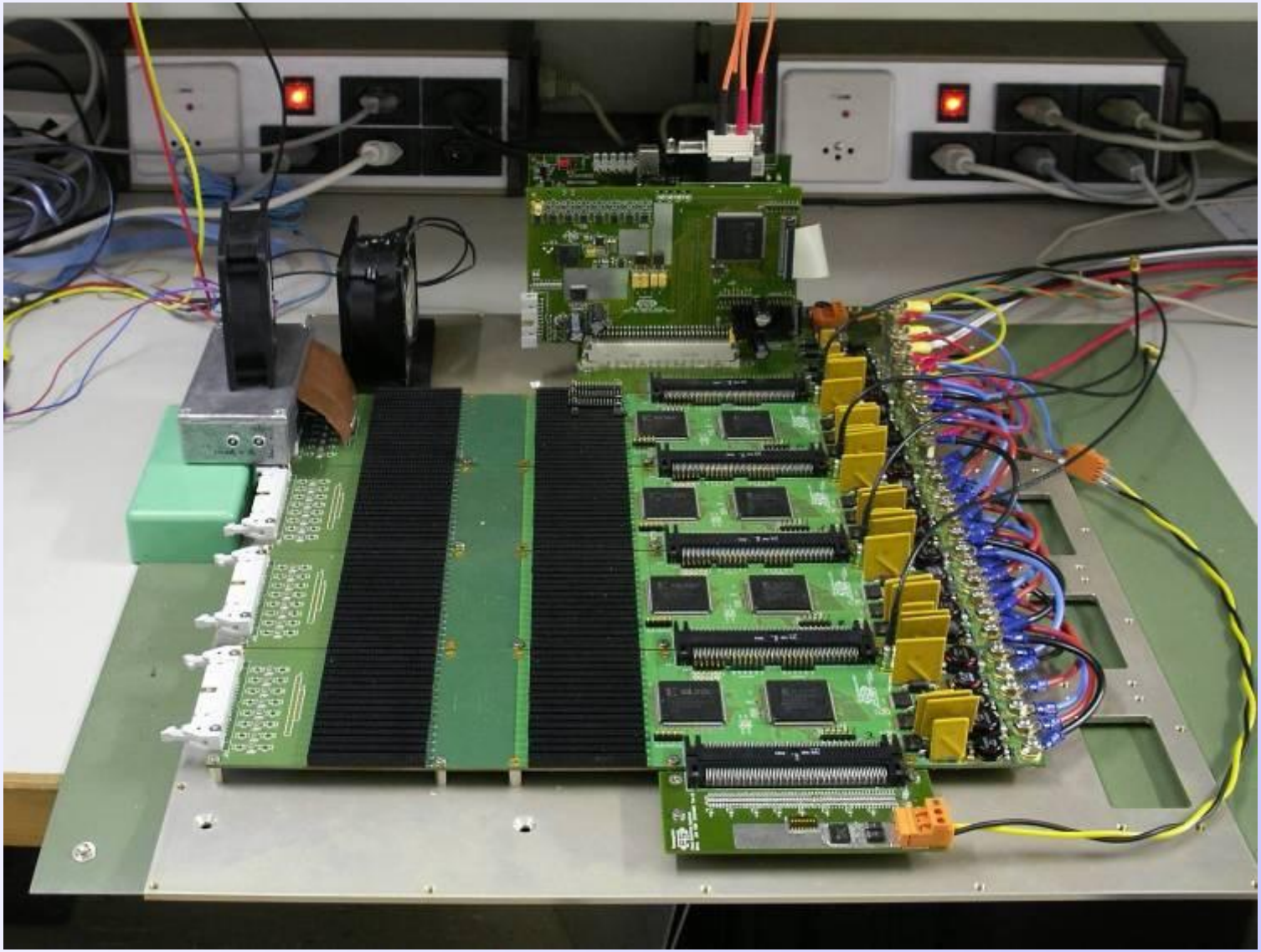
Main-board

- Main-board
  - *16 × front end PCBs*
  - *Spartan 3 FPGA*
  - *Independent read-out for each FE*
  - *20 event FIFO for each FE*
  - *12 µs parallel transfer to GigaSTaR*
  - *max. through put 83.3 kevents per sec*
  - *multiplexed test pulse output*
  - *5x free programmable interconnection signals*
  - *up to 16 MB = 256 spectroscopic channels*

Event structure

No	31(MSB) (LSB)0
1	Event state (16bit) | Event type (8bit) | FE no (8 bit)
2	Alpha ADC conv. time (16bit) | Alpha ADC (16bit)
3	Fiss ADC conv. time (16bit) | Fiss ADC (16bit)
4	Thresh. Time 1 (16bit) | Thresh. Time 0 (16bit)
5	Thresh. Time 3 (16bit) | Thresh. Time 2 (16bit)
6	Thresh. Time 5 (16bit) | Thresh. Time 4 (16bit)
7	Thresh. Time 7 (16bit) | Thresh. Time 6 (16bit)
8	Thresh. Time 9 (16bit) | Thresh. Time 8 (16bit)
9	Thresh. Time 11 (16bit) | Thresh. Time 10 (16bit)
10	Thresh. Time 13 (16bit) | Thresh. Time 12 (16bit)
11	Thresh. Time 15 (16bit) | Thresh. Time 14 (16bit)
18	Beam counter (32bit)
19	I/O state (16bit) | Beam counter (16bit)
20	Time stamp (32bit)
21	nn (8bit) | ss (8bit) | Time stamp (16bit)
22	yy (8bit) | mm (8bit) | dd (8bit) | hh (8bit)

PC interface / DAC pulser



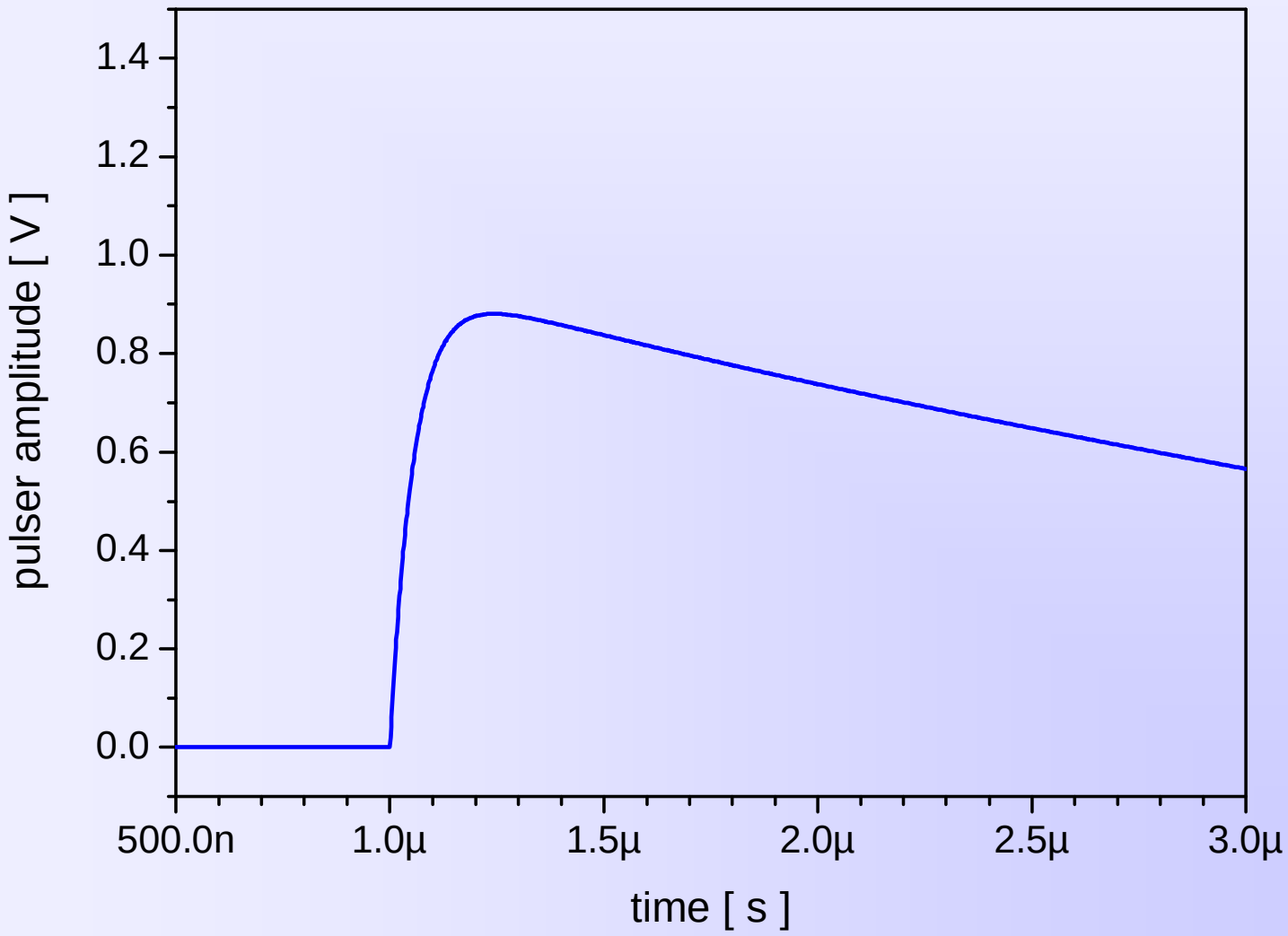
PC interface / DAC pulser

Event interface to PC

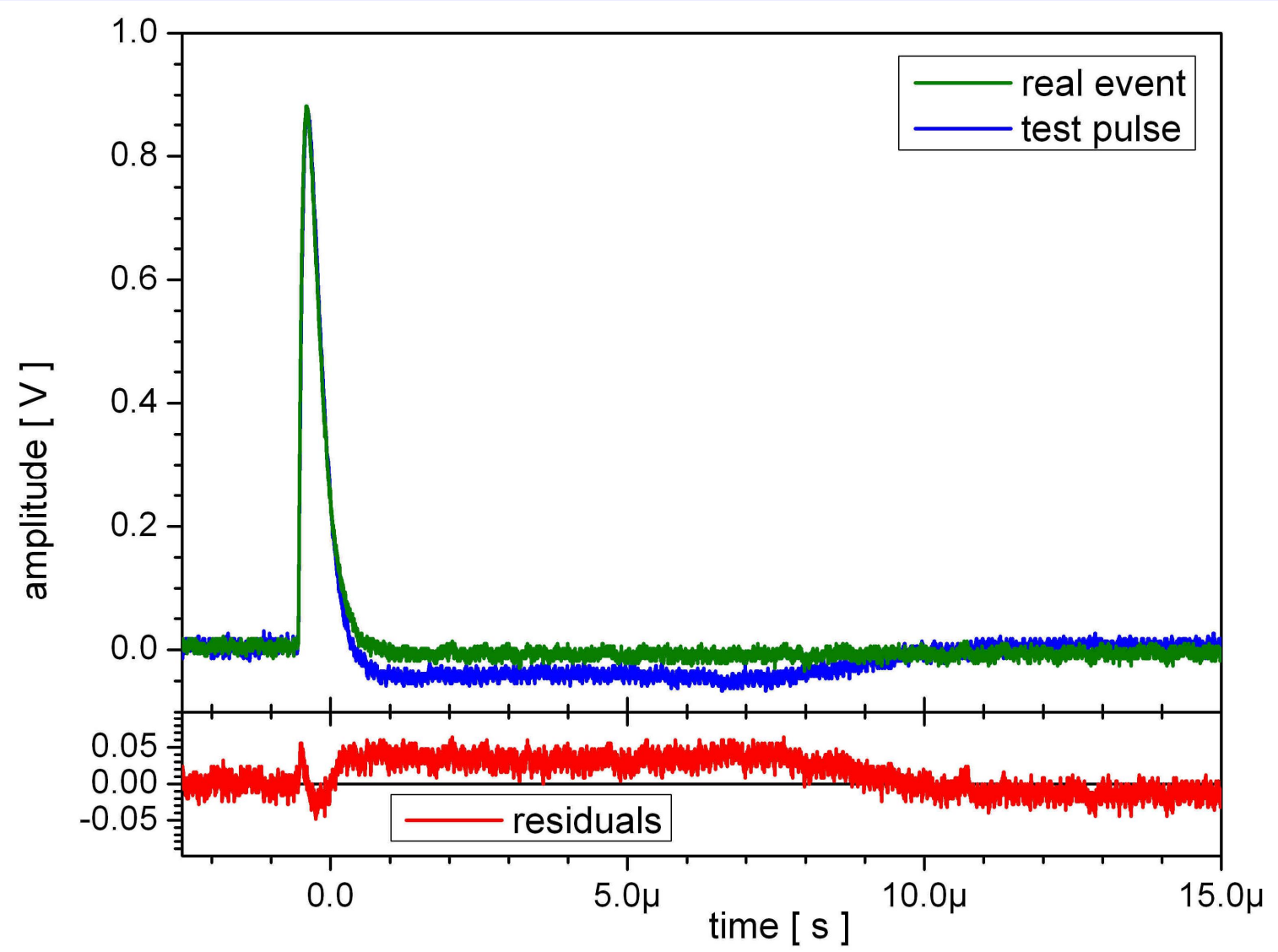
- *Inova GigaSTaR point to point connection*
- *1.32 GBit/s via fiber optics*
- *4096 event FIFO*
- *max. through put 1.85 Mevents per sec*

- DAC test pulse generator
  - *Fujitsu* MB86064 14-bit 800 MSamlpes/s DAC
  - *2* × free programmable waveforms up to 20.48 *µs*
  - *adjustable reference voltage via 8 bit DAC*

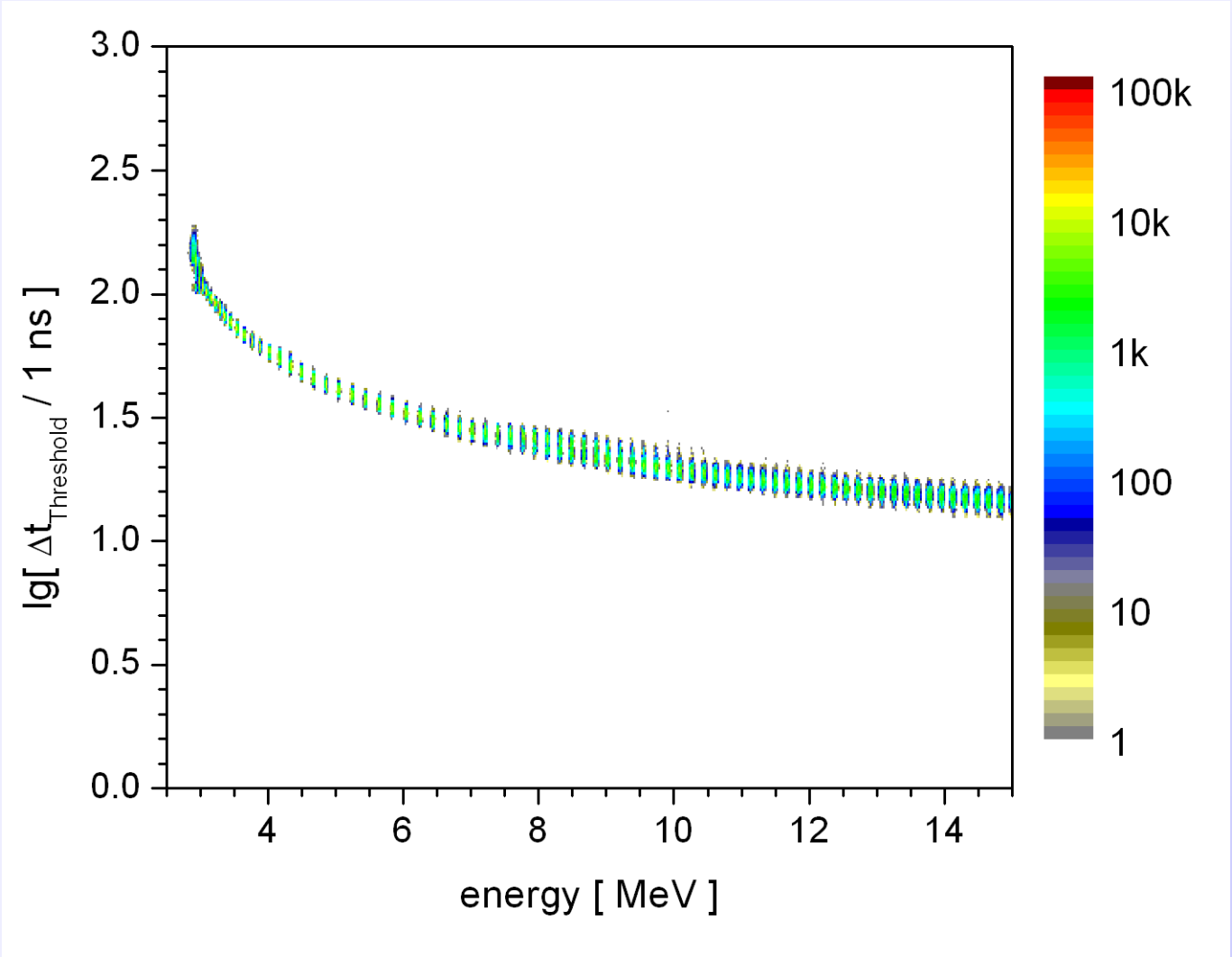
Wave-form for pure α event



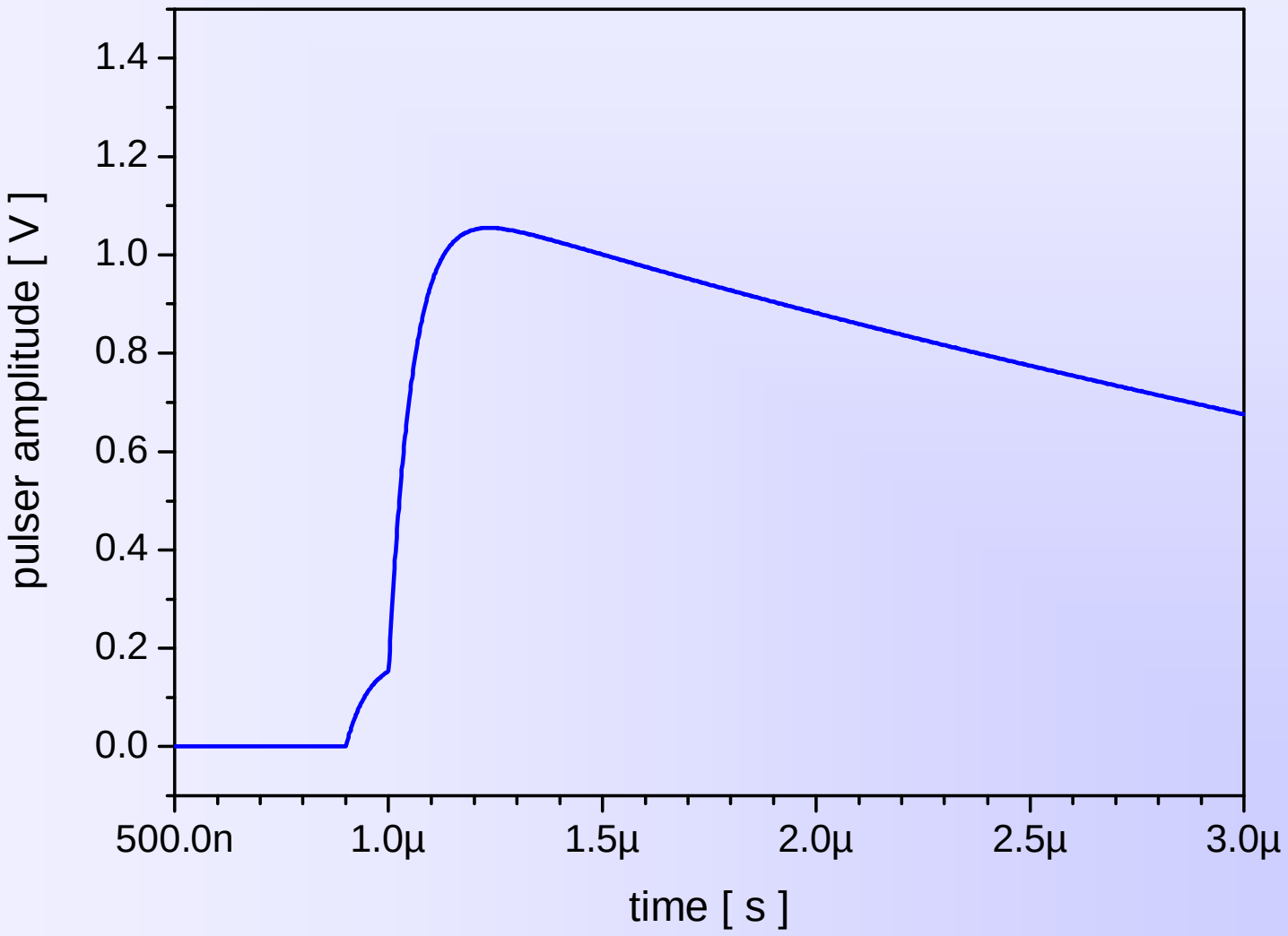
Pulser response vs. real α signal



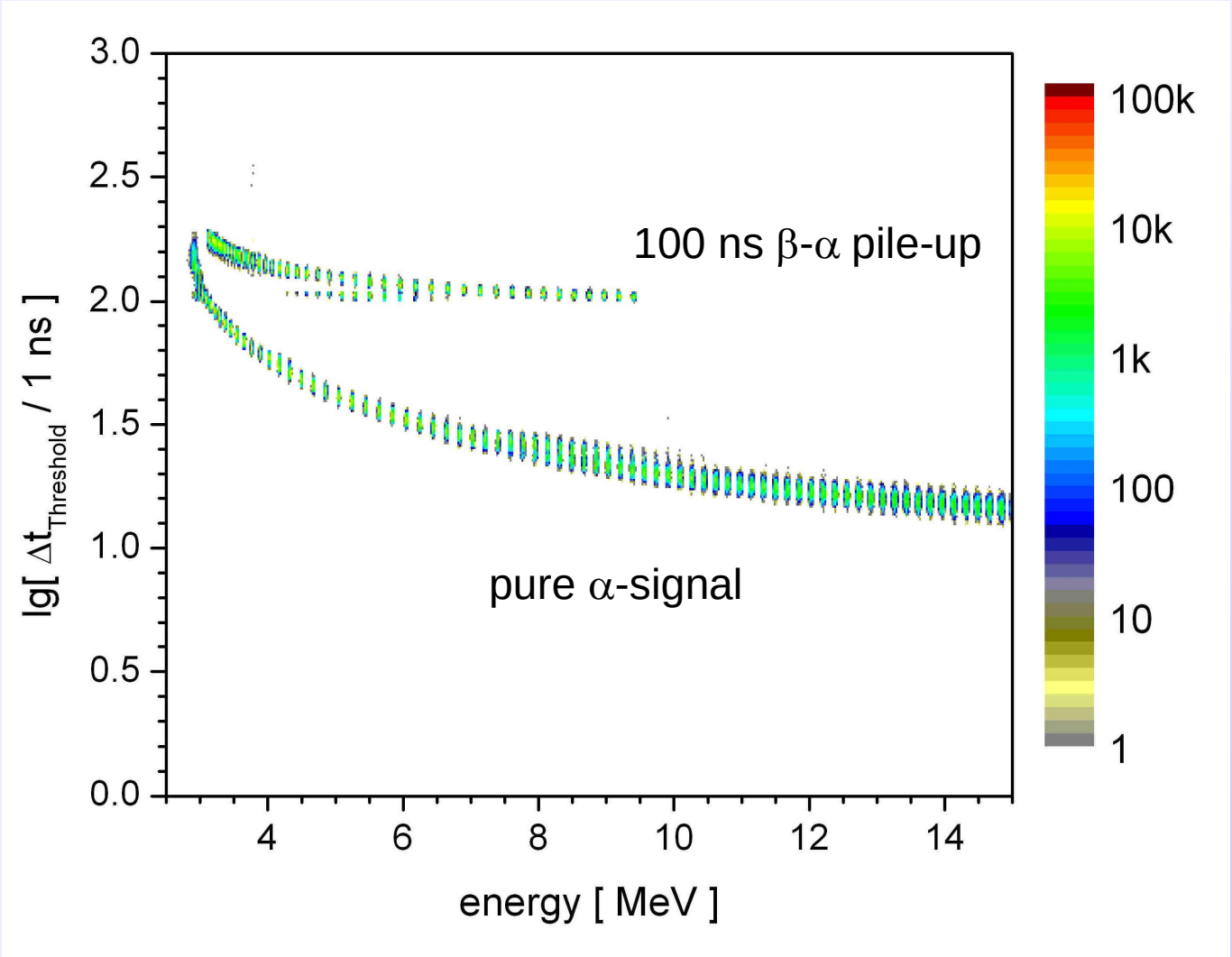
Pulser energy scan



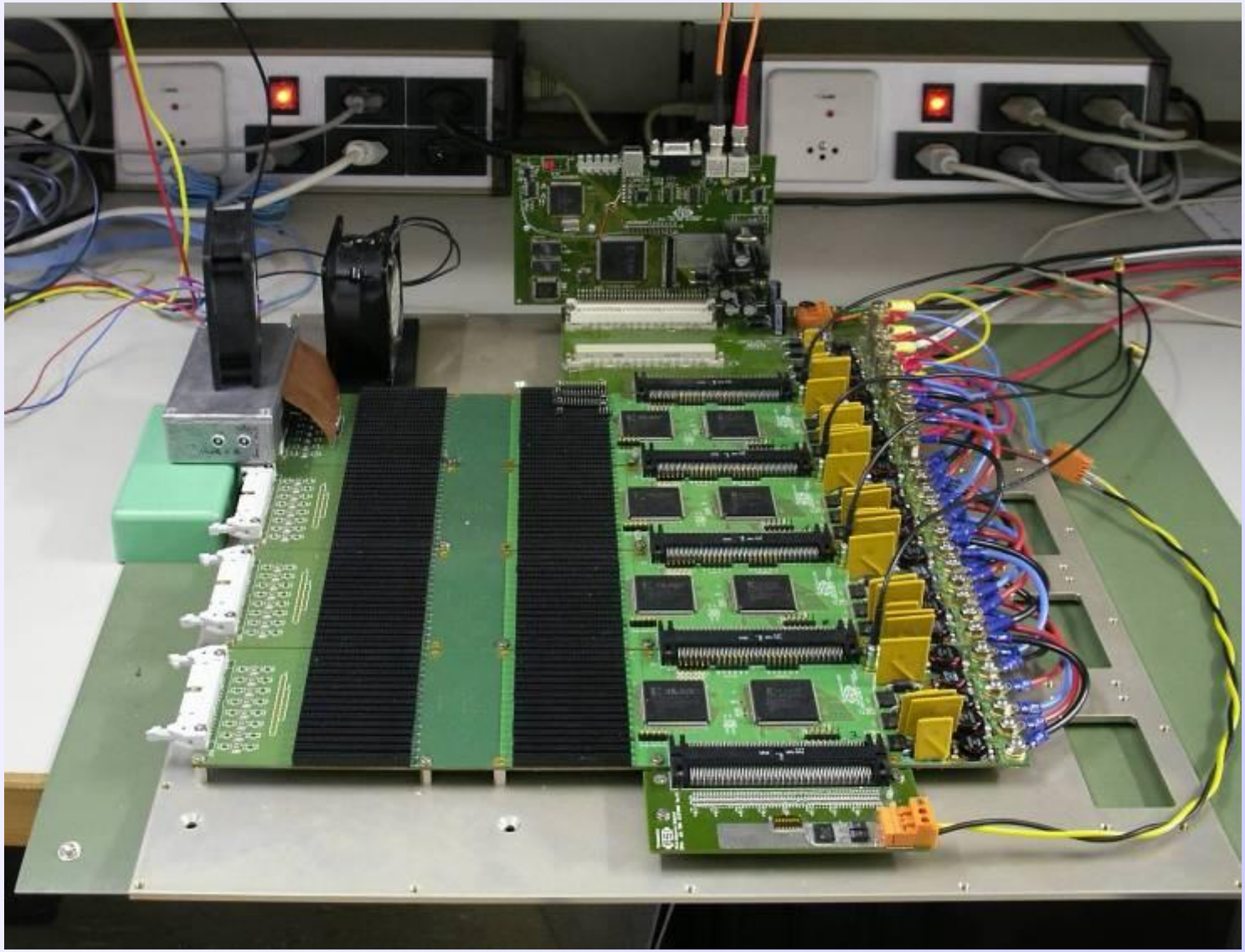
Wave-form for 100 ns β-α pile-up



Pulser pile-up scan



Micro controller unit

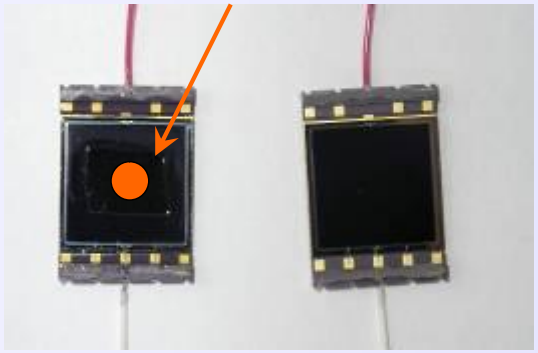


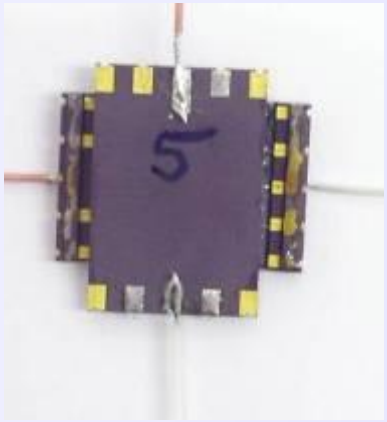
Micro controller unit

- Motorola MC68HC12
  - *16 MHz clock, 32 kByte RAM*
  - *512 MB Compact Flash Memory*
  - *control start up phase of FPGAs and comparators*
  - *each MB or FE FPGA independently configurable*
  - *256 × firmware configurations for MB and FE FPGAs on CF*
  - *256 × threshold settings for all FE comparators on CF*
  - *Control DAC test pulse generator*
  - *256 × wave-forms on CF*
  - *communication with PC via serial ports*
    RS-232 copper, fiber optics or USB 1.1

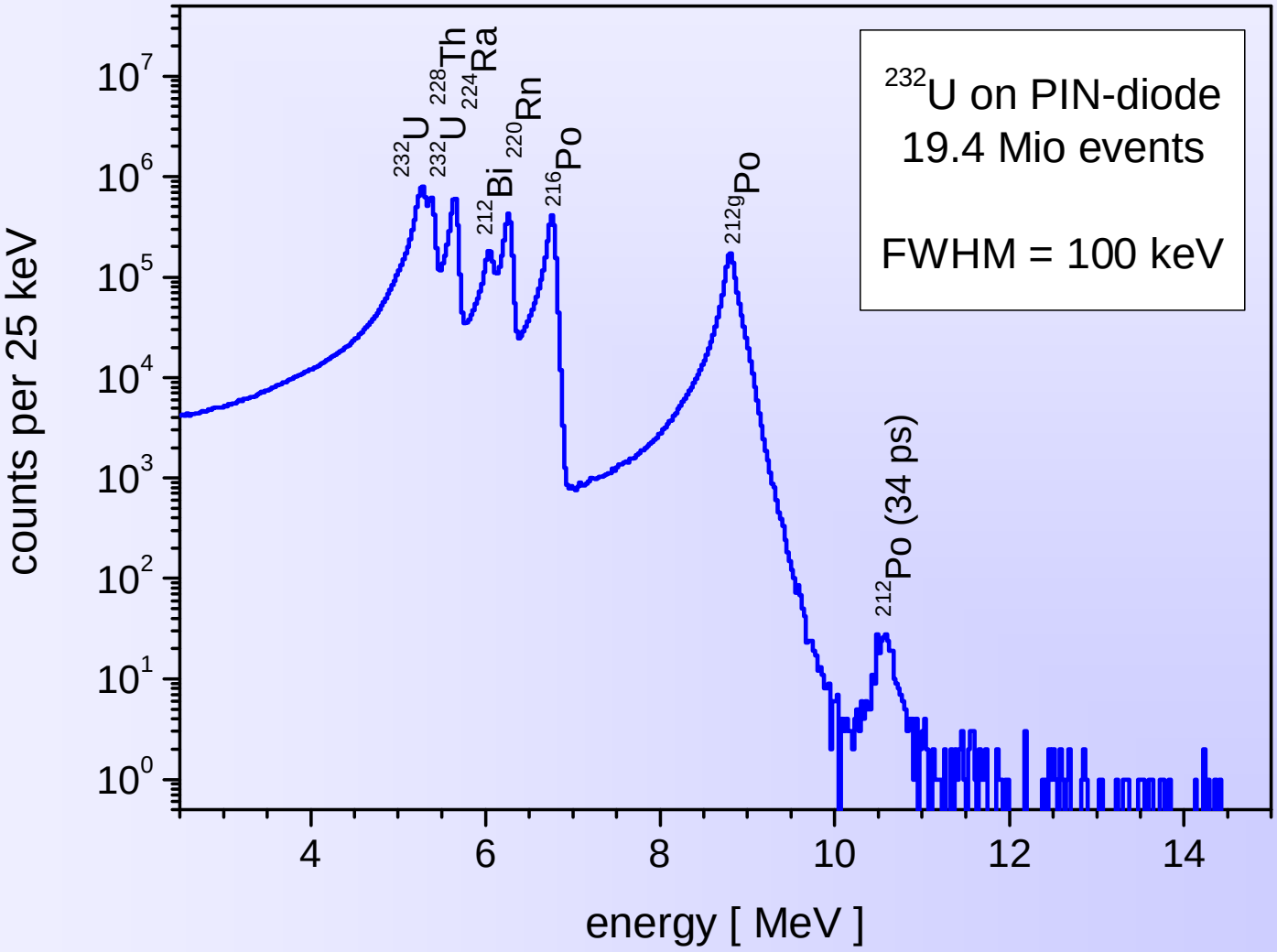
First measurements

^{232}U

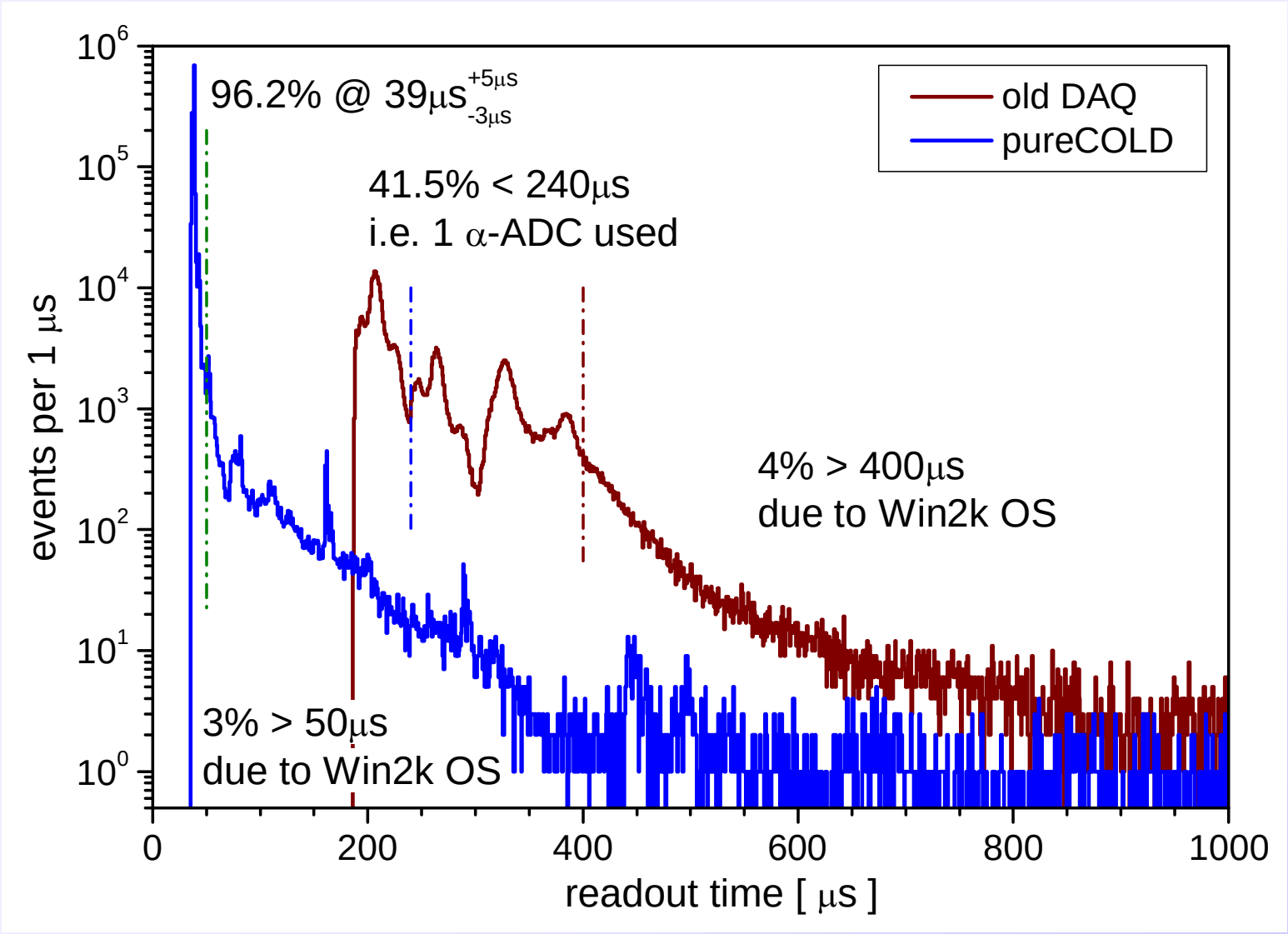




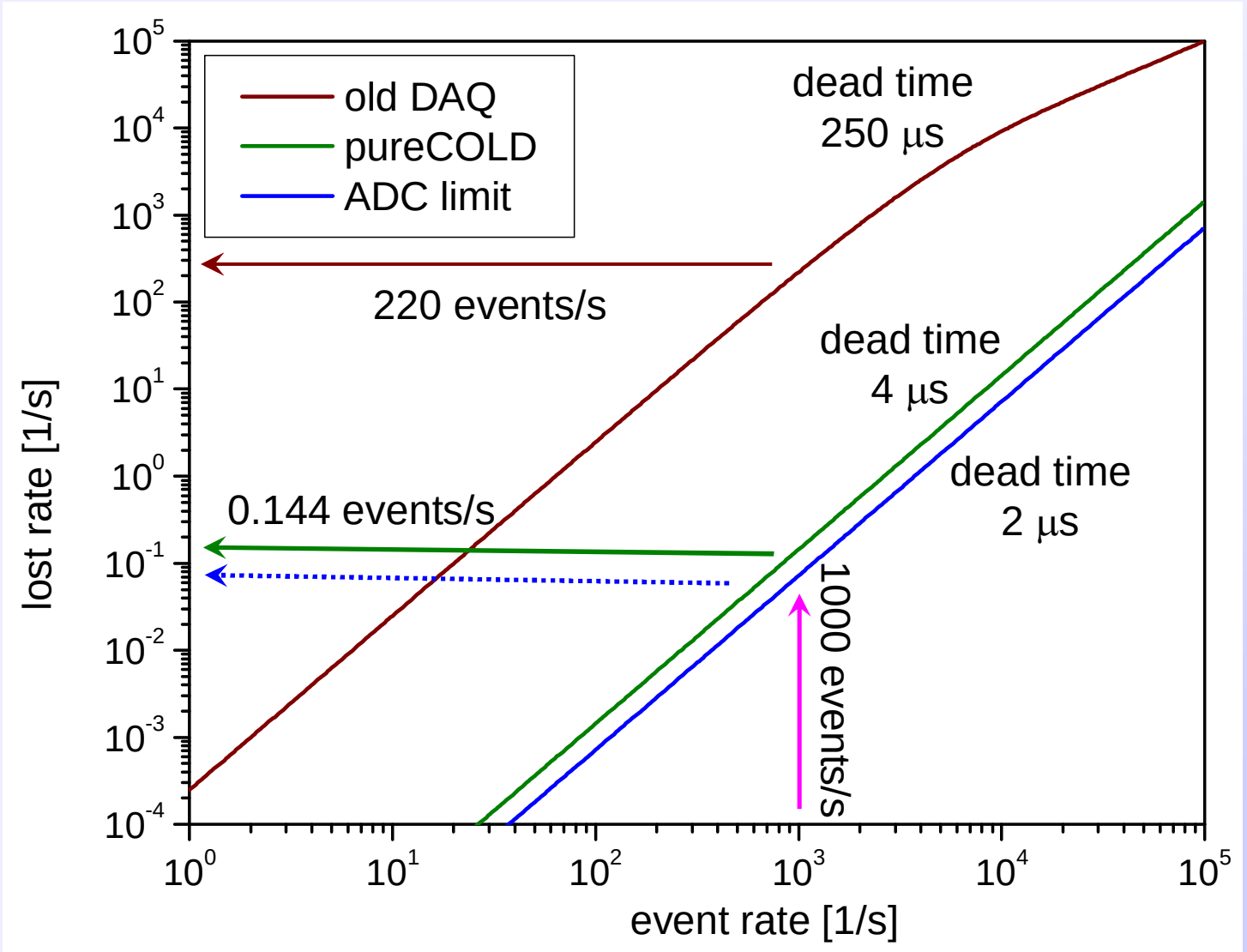
^{232}U - spectrum



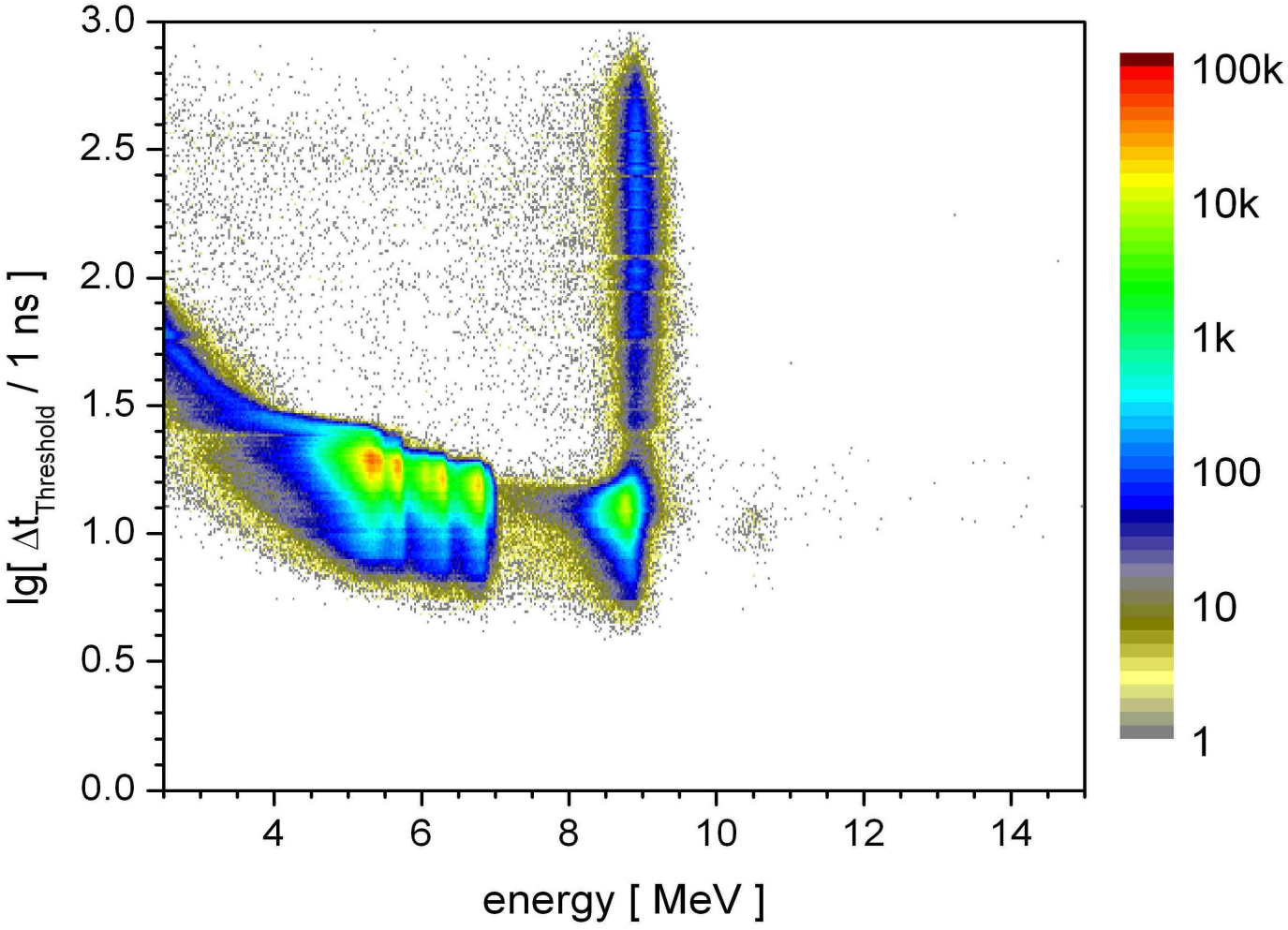
Readout time spectrum



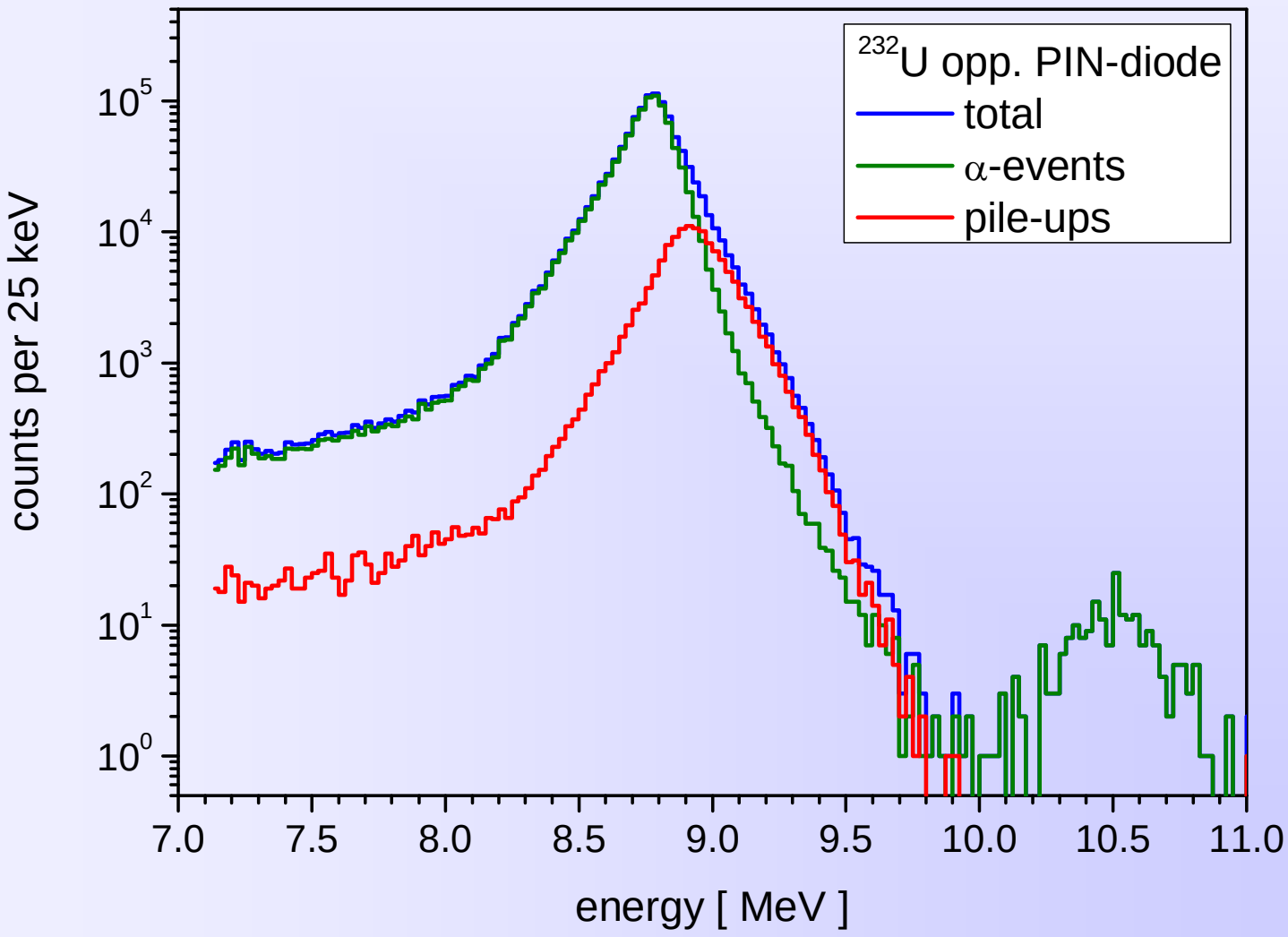
Event lost rate



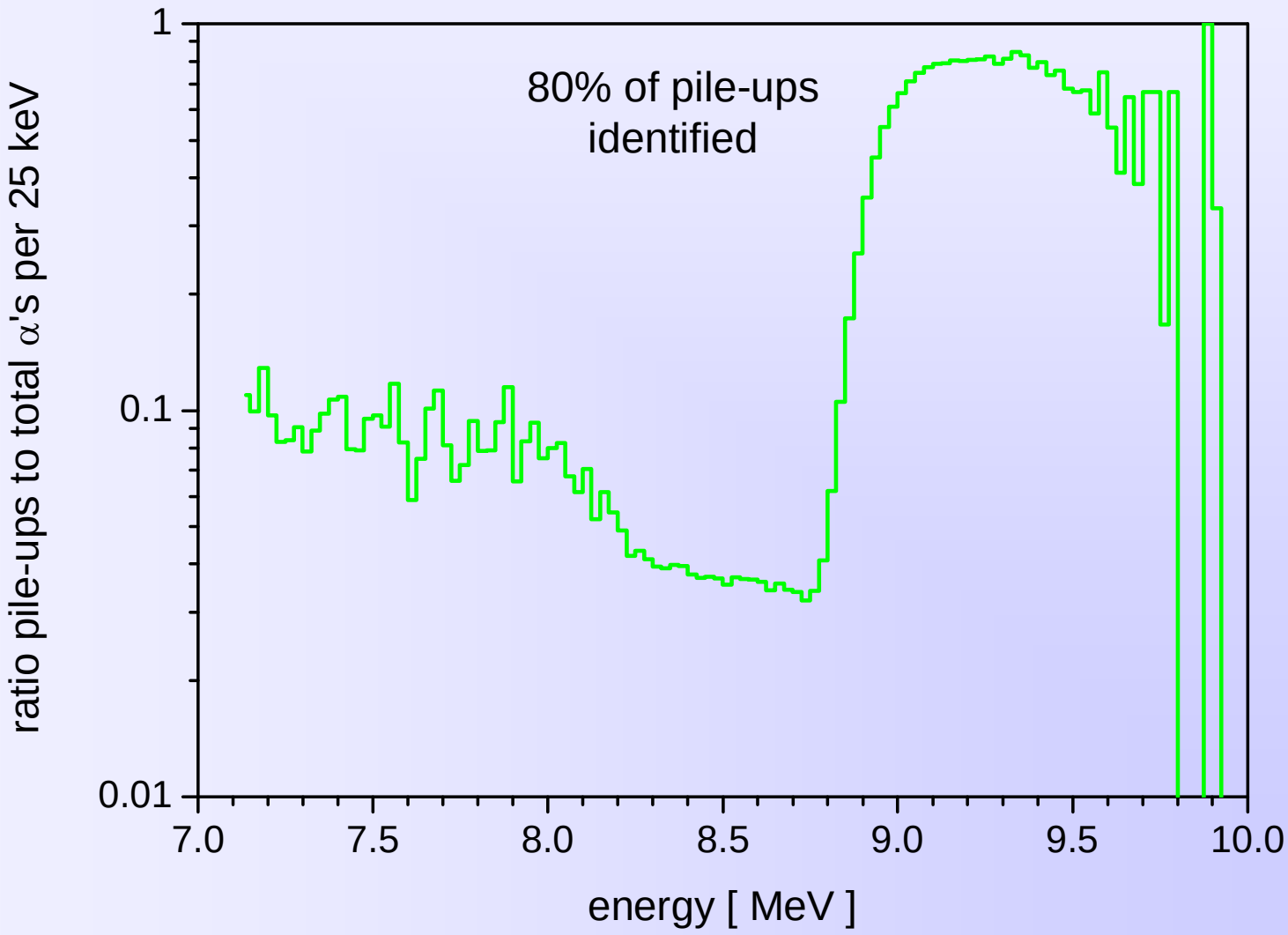
^{232}U time vs. α spectrum



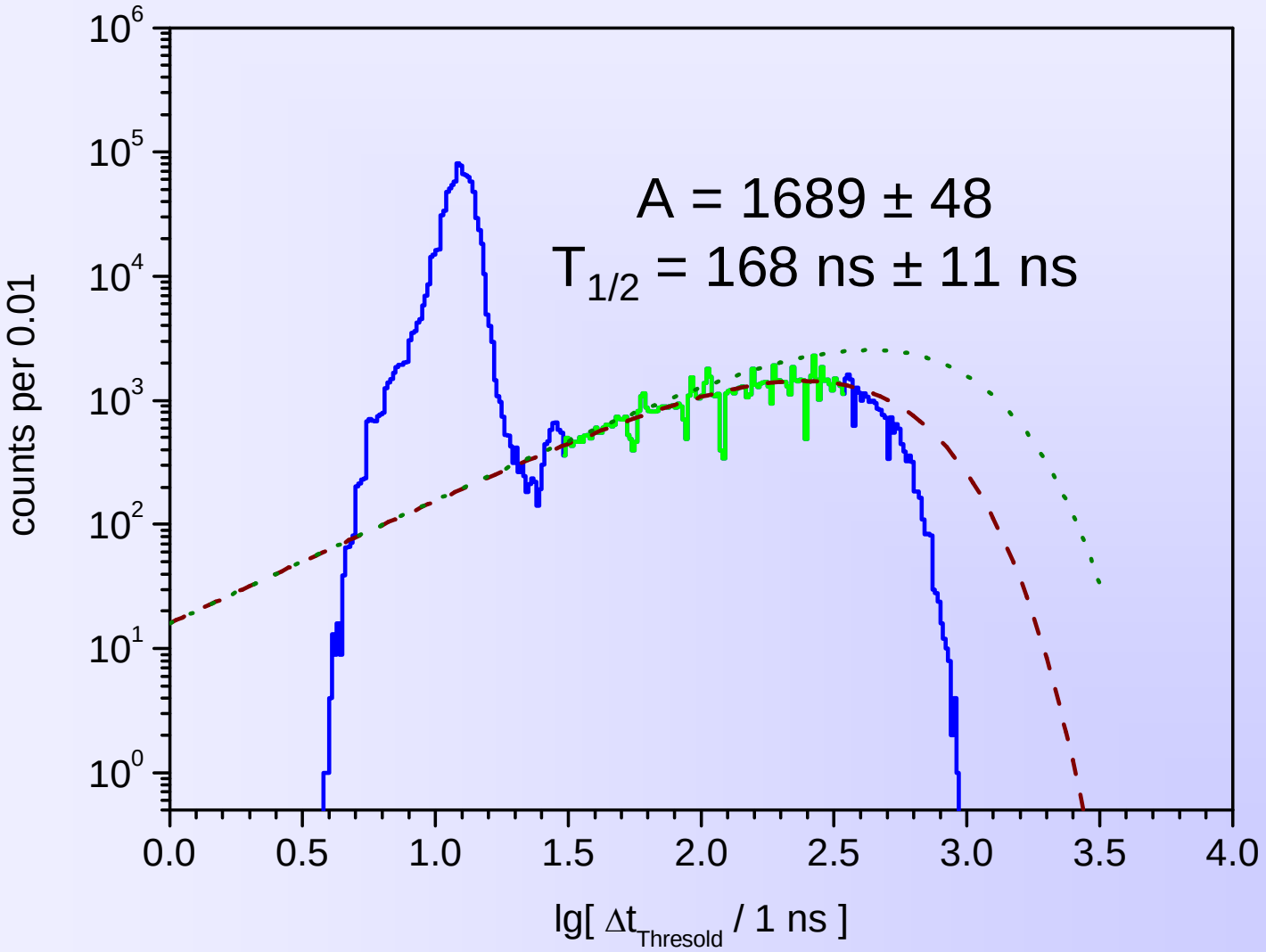
Pile-up detection



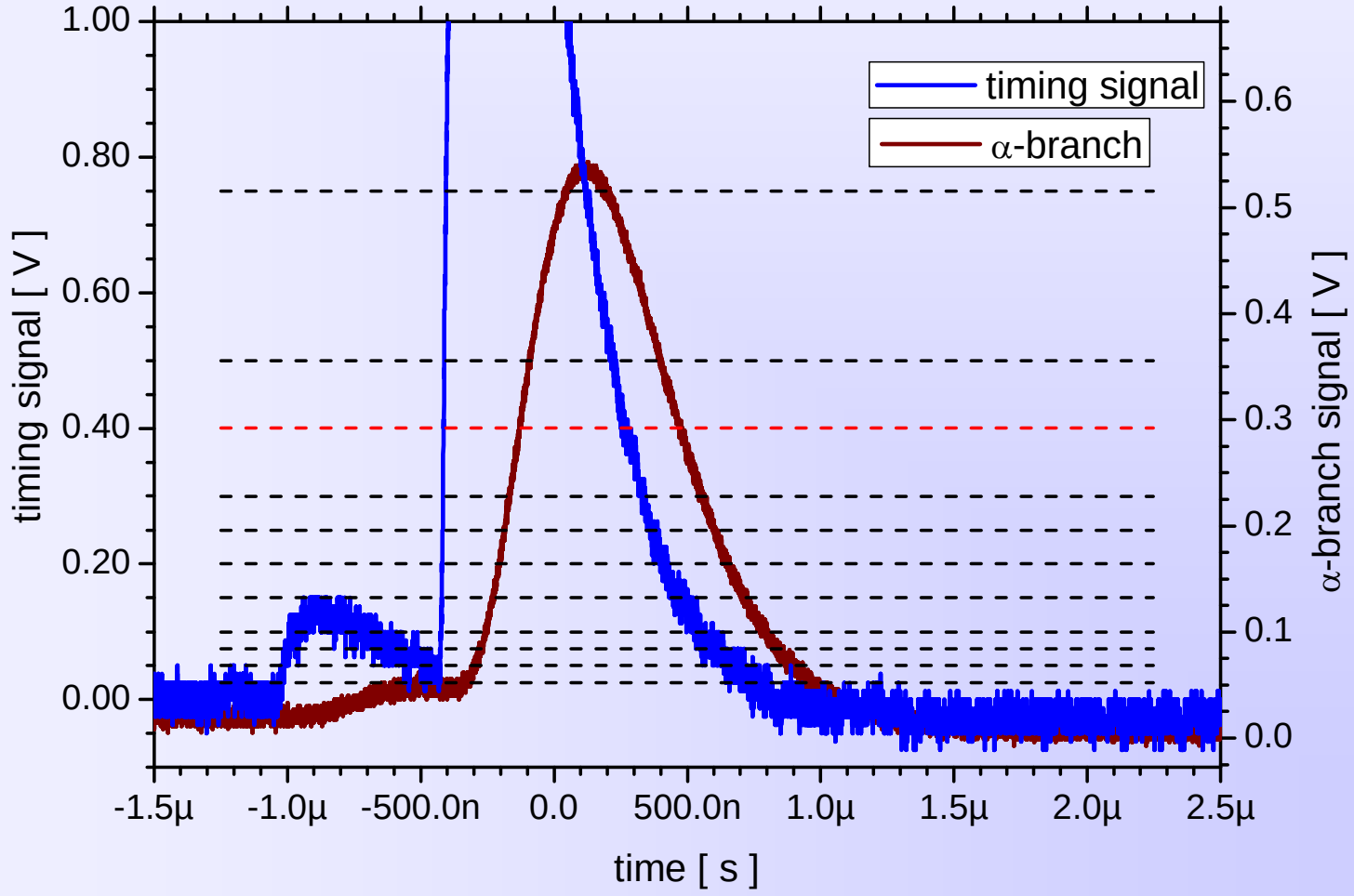
Pile-up detection



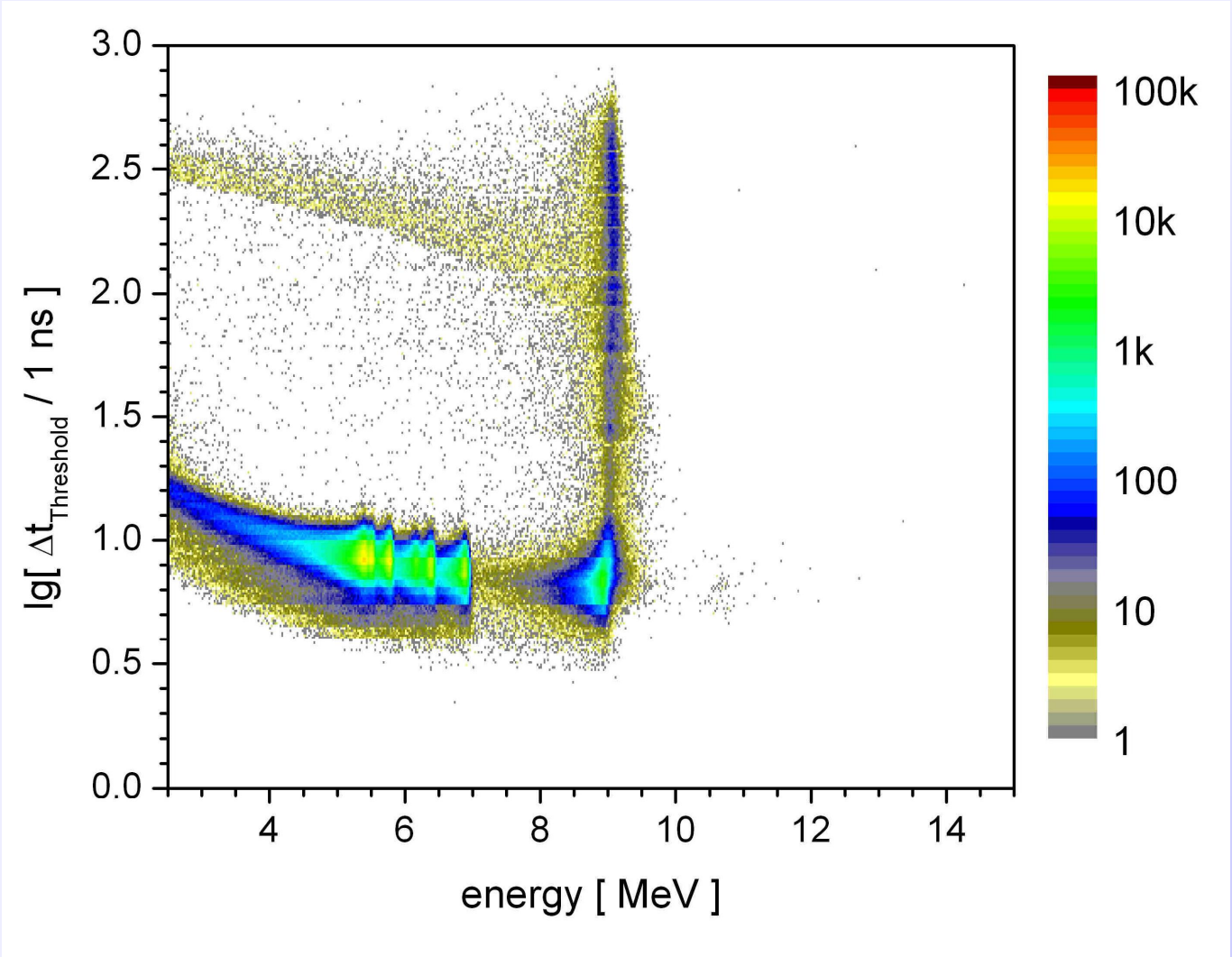
Half-live of ^{212}Po



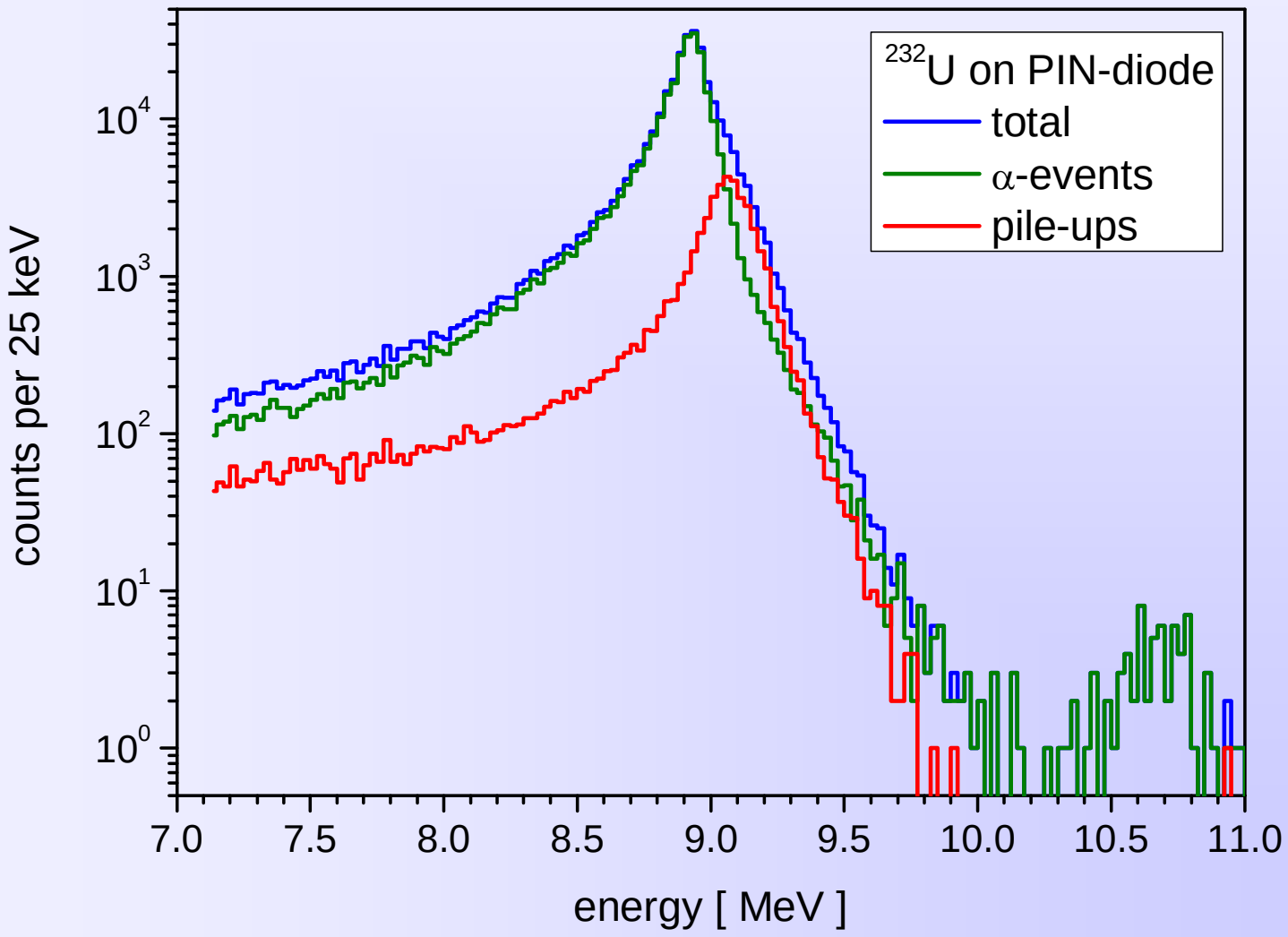
Working principle



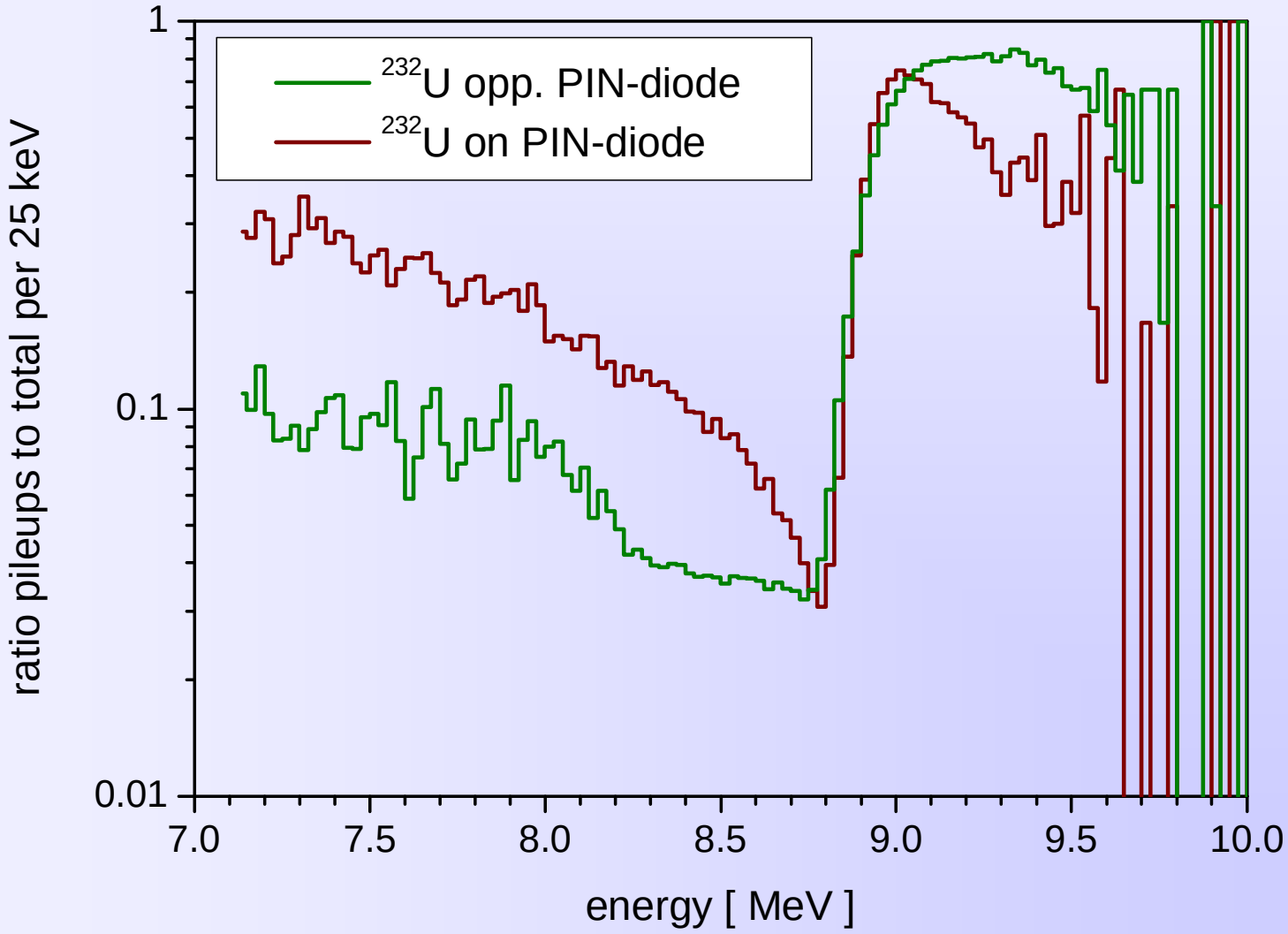
^{232}U on PIN-diode



Pile-up detection



Pile-up detection



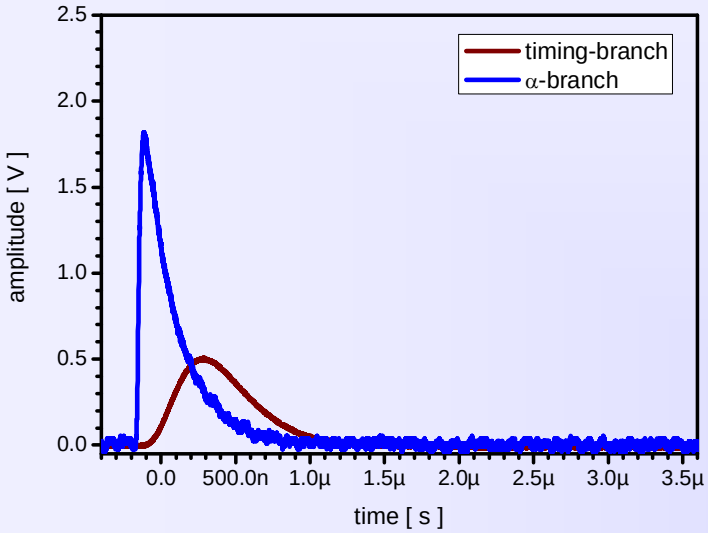
Outlook

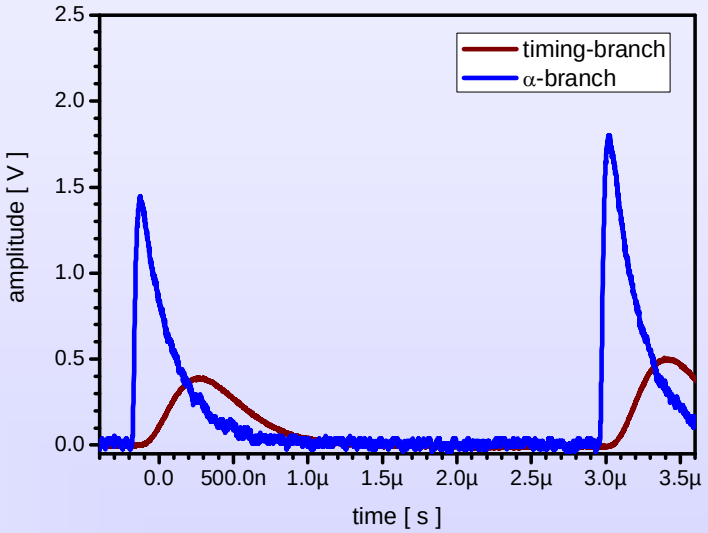
- good spectroscopic behavior in table-top tests
  - *4 µs minimal time between events*
  - *FWHM ≈ 100 keV*
  - *pile-up identification ≈ 80%*
- 80 × FE modules manufactured
- 5 × MB modules manufactured

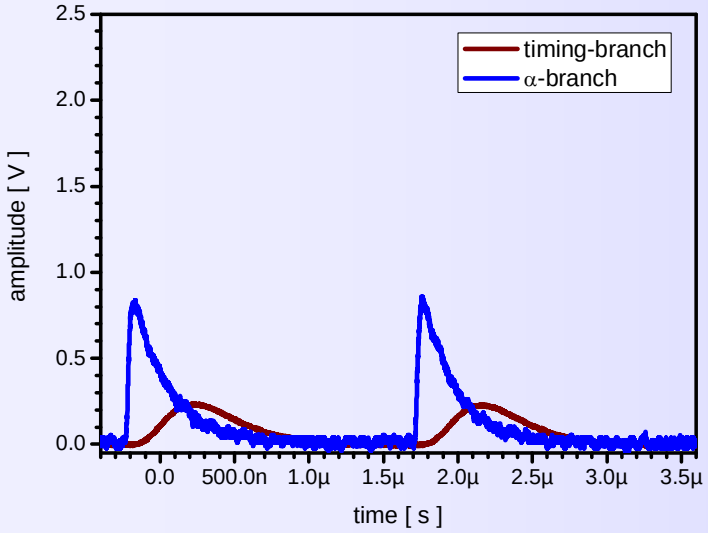
Outlook

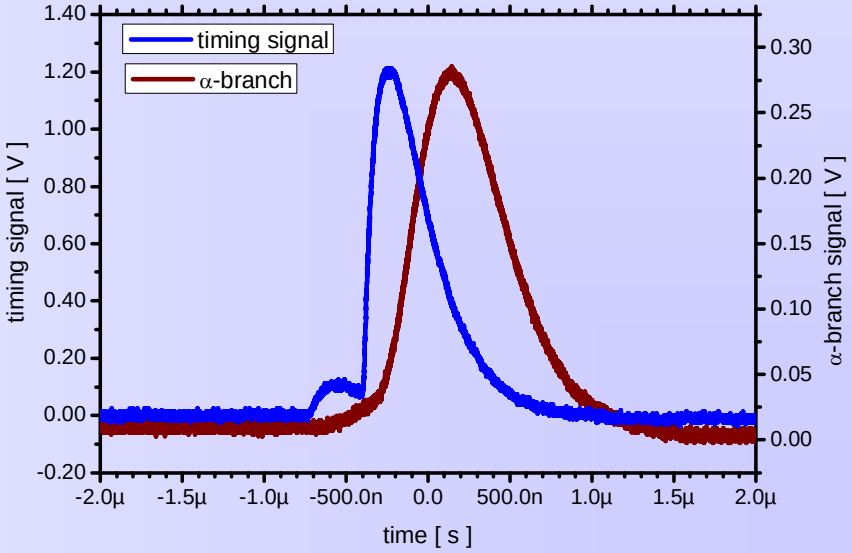
- Power-supply for 64 FE ready
- Tests with 4 full equipped MB = 64 FE
- Tests with COLD detector-bar
- Improvements of FPGA configurations
  - *Fast counter implementation*
    E. Koutroulis, A. Dollas, K. Kalaitzakis: "High-frequency pulse width modulation implementation using FPGA and CPLD ICs": J. of Systems Architecture 52 (2006) 332–344
  - *Complex trigger logic*

Processable events

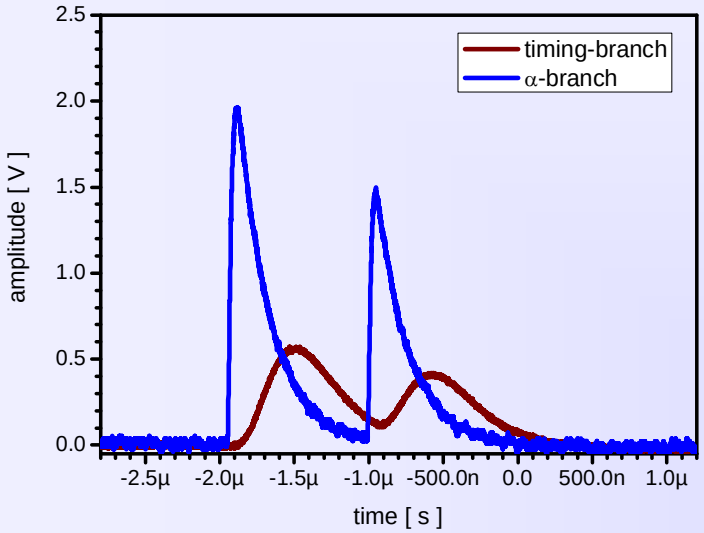


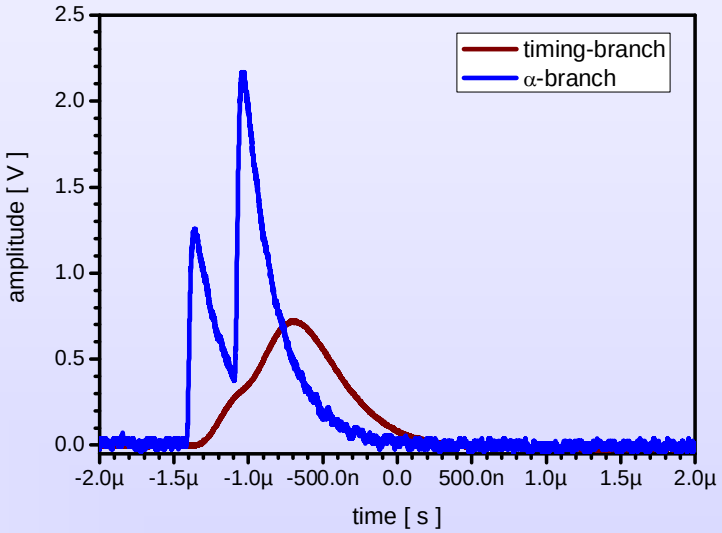


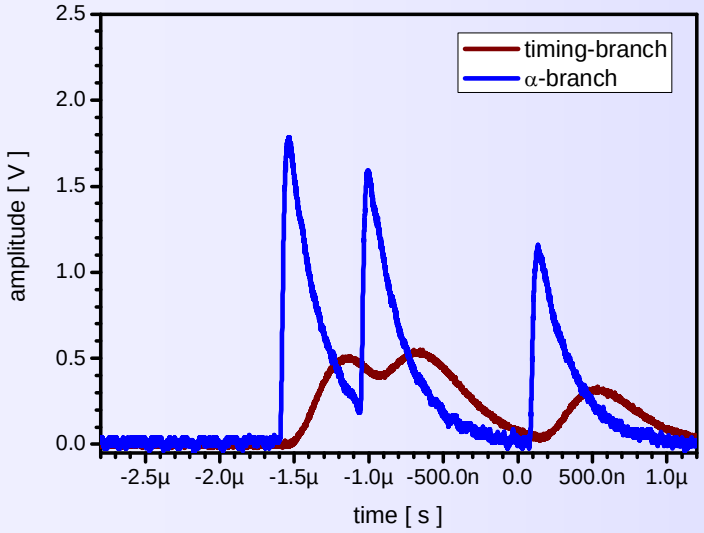


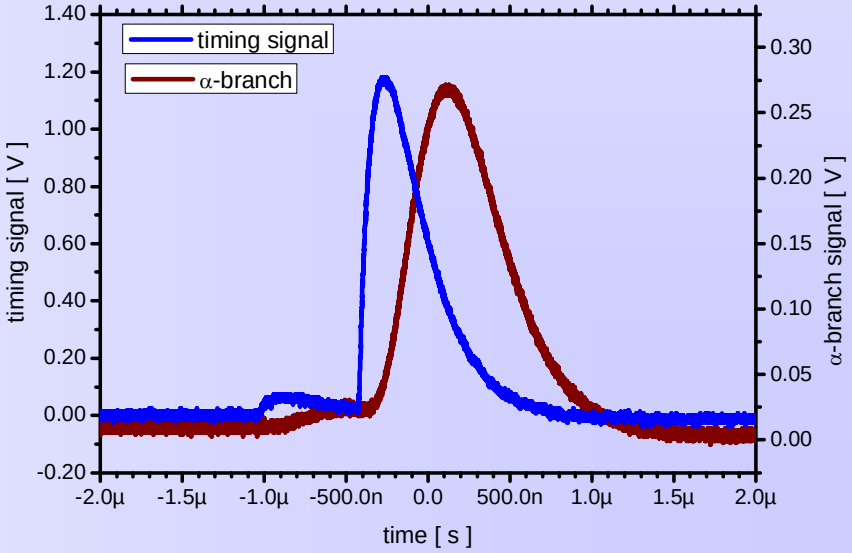


Possible cases









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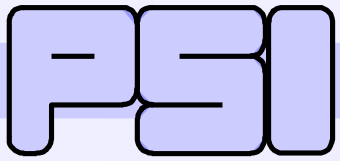
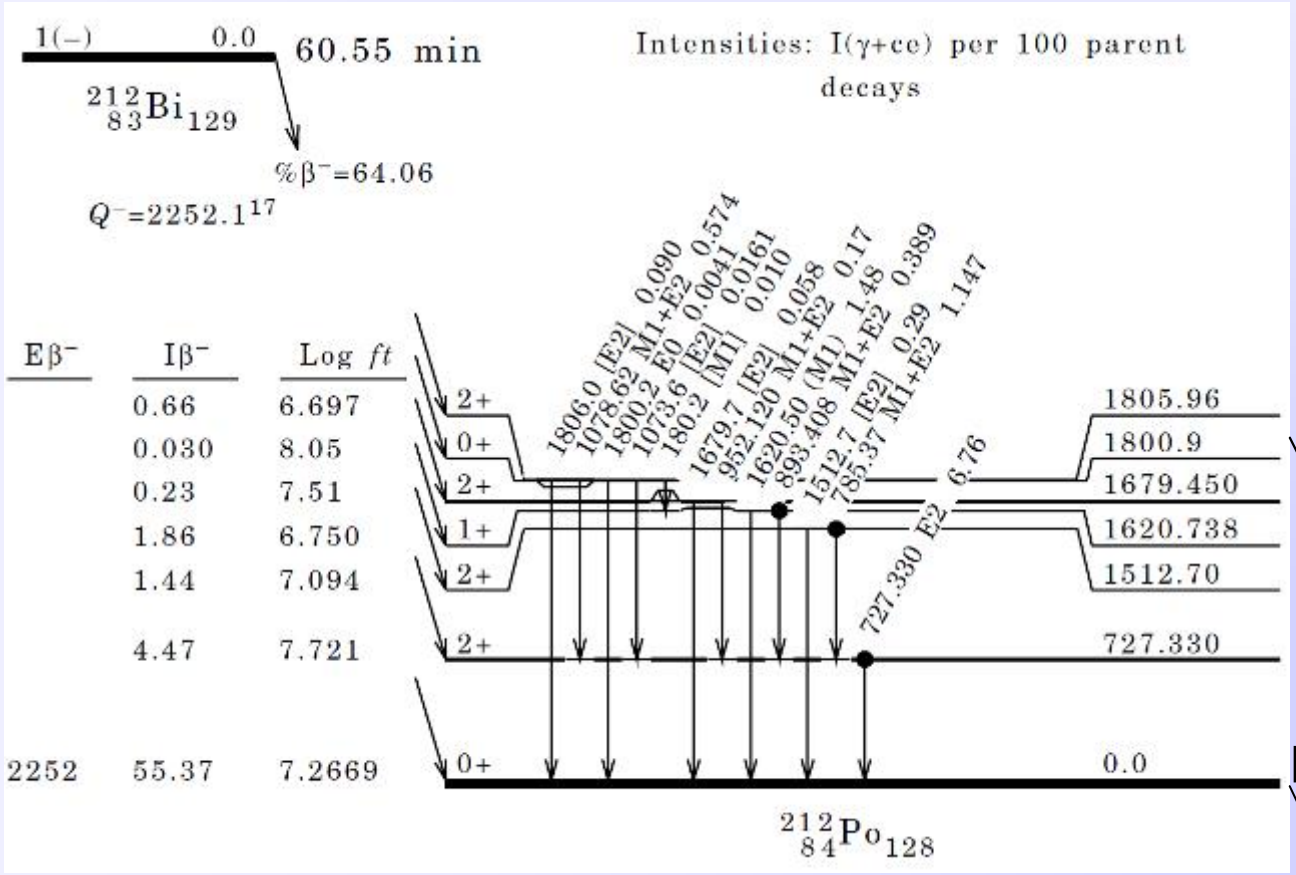


Thank you for your attention

Decay schema of ^{212}Bi



E_α=10.554 MeV
(34 ps life-time)
>0.01%

E_α=8.78486 MeV
100%

E. Brown: Nuclear Data Sheets 104 (2005) 427-496