

# Optical Networks On Chip: Enabling Future Memory

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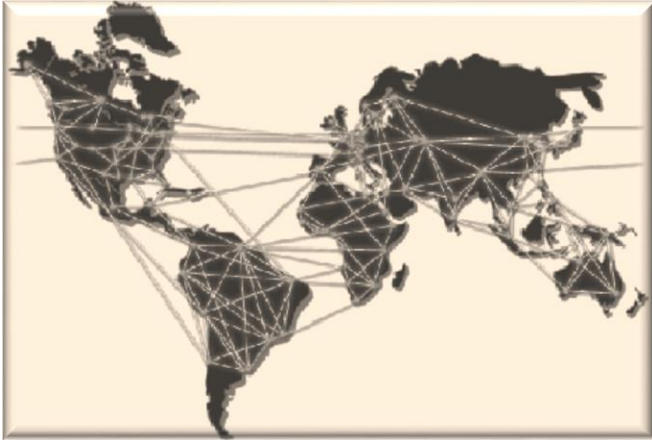
Department of Engineering



# WHY OPTICAL NETWORKS ON CHIP?



# Optical networks are already connecting us



1980s our countries...

... datacenters and cities



1990s our homes

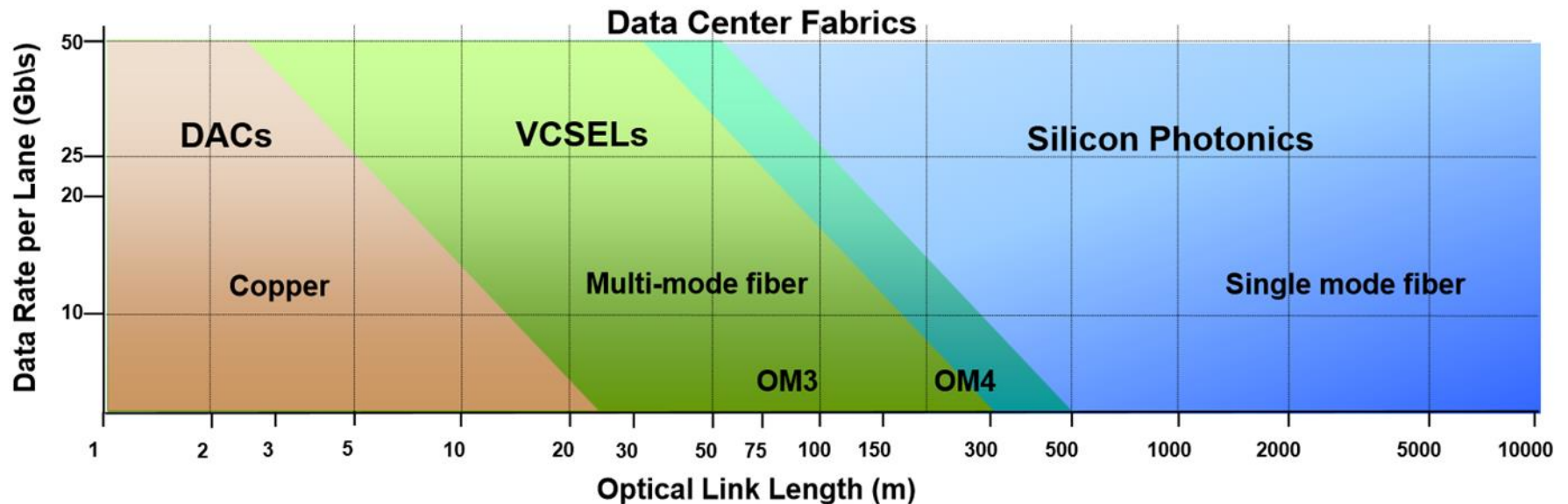


2000s our computers



# There is a trade-off of length vs. bandwidth

## Mellanox View of 100G Data Center Fabrics



### Direct Attach Copper

- Zero power
- Demo'd 8m at 100G
- Best fit 3m

### Active Optical Cables

- VCSELs or SiP
- Reaches to 200m
- Best fit for 5-20m

### VCSEL Transceivers

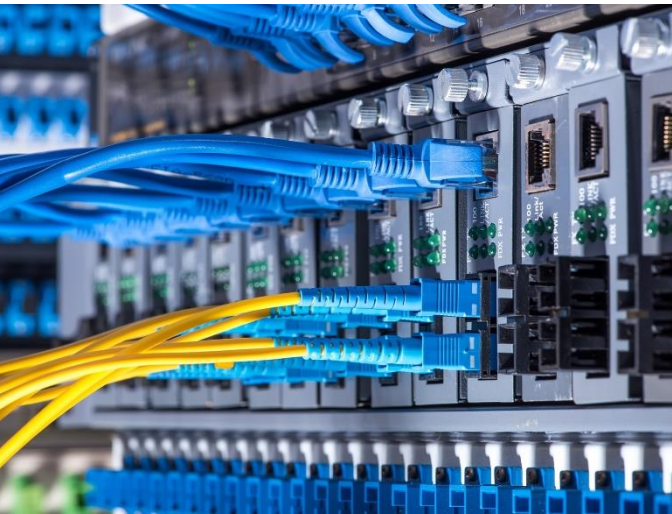
- Reaches to 100m
- Best fit for MMF

### SiP Transceivers

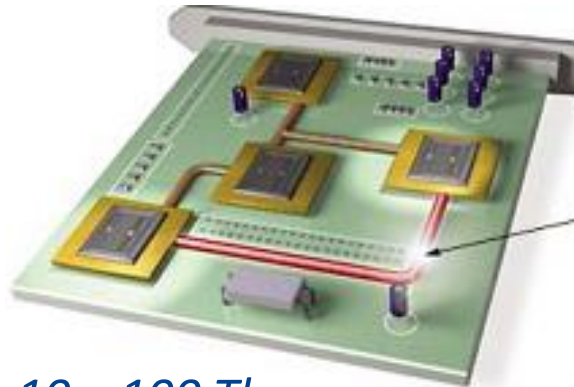
- Reaches to 2km
- Best fit for SMF
- Parallel or WDM

# Optical interconnects for increasingly smaller distances, driven by bandwidth requirements

**Today – commercial**  
Optical connections in data centers



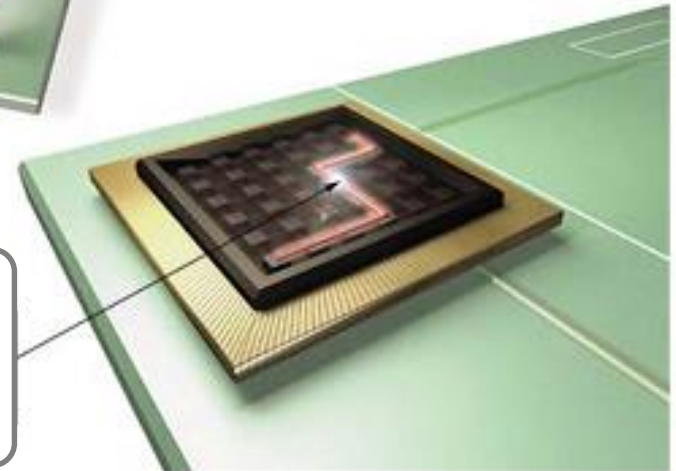
*Near future: 1 Tbps...*



**Today – commercial**  
Optical connections in/on boards

*... 10s -100 Tbps...*

**Future**  
Optical interconnects on processor (?)



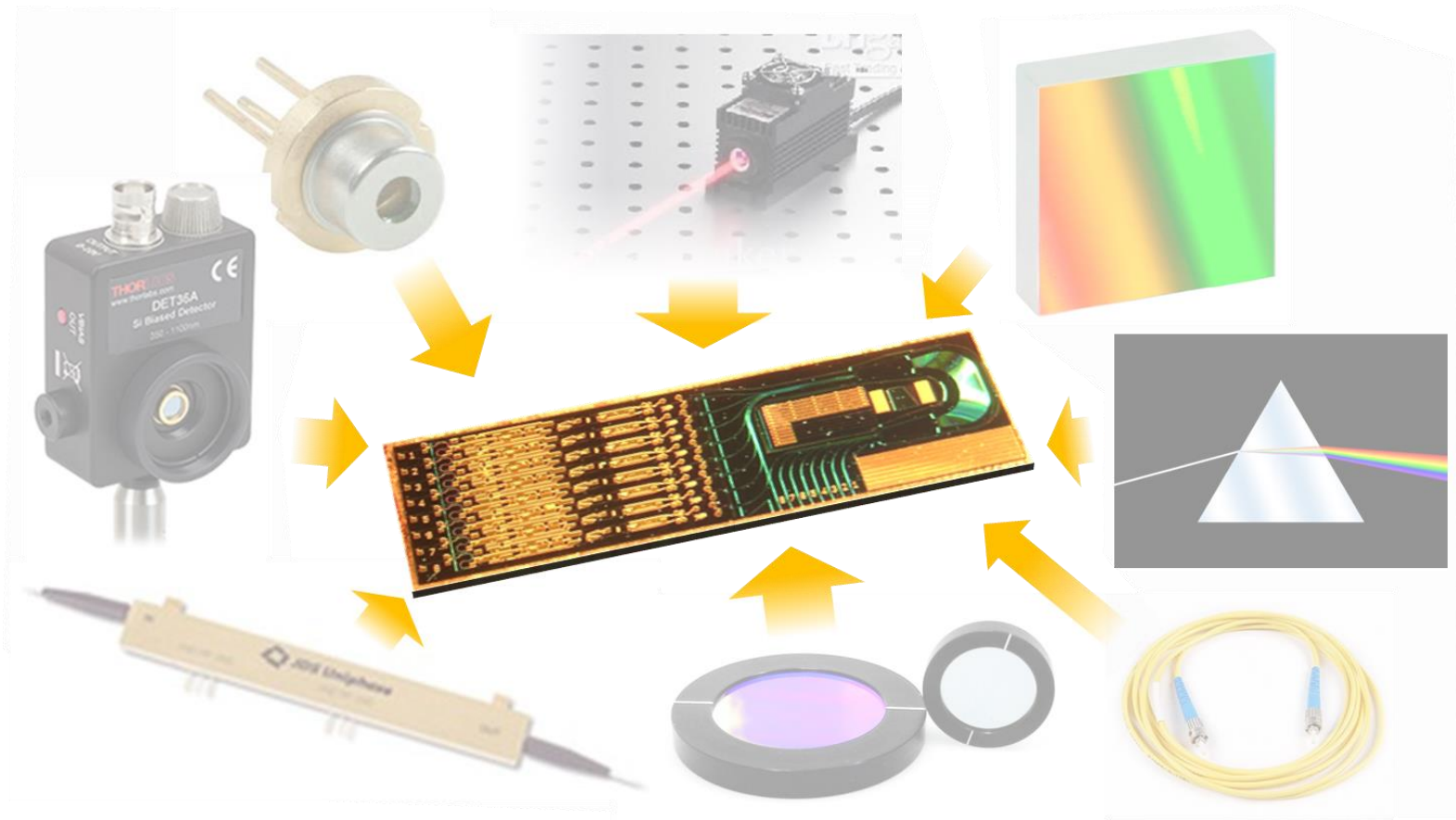
*... 500 Tbps*

*D. A. B. Miller, Proc. IEEE 97, 7 (2009)*

# HOW OPTICAL NETWORK ON CHIP?

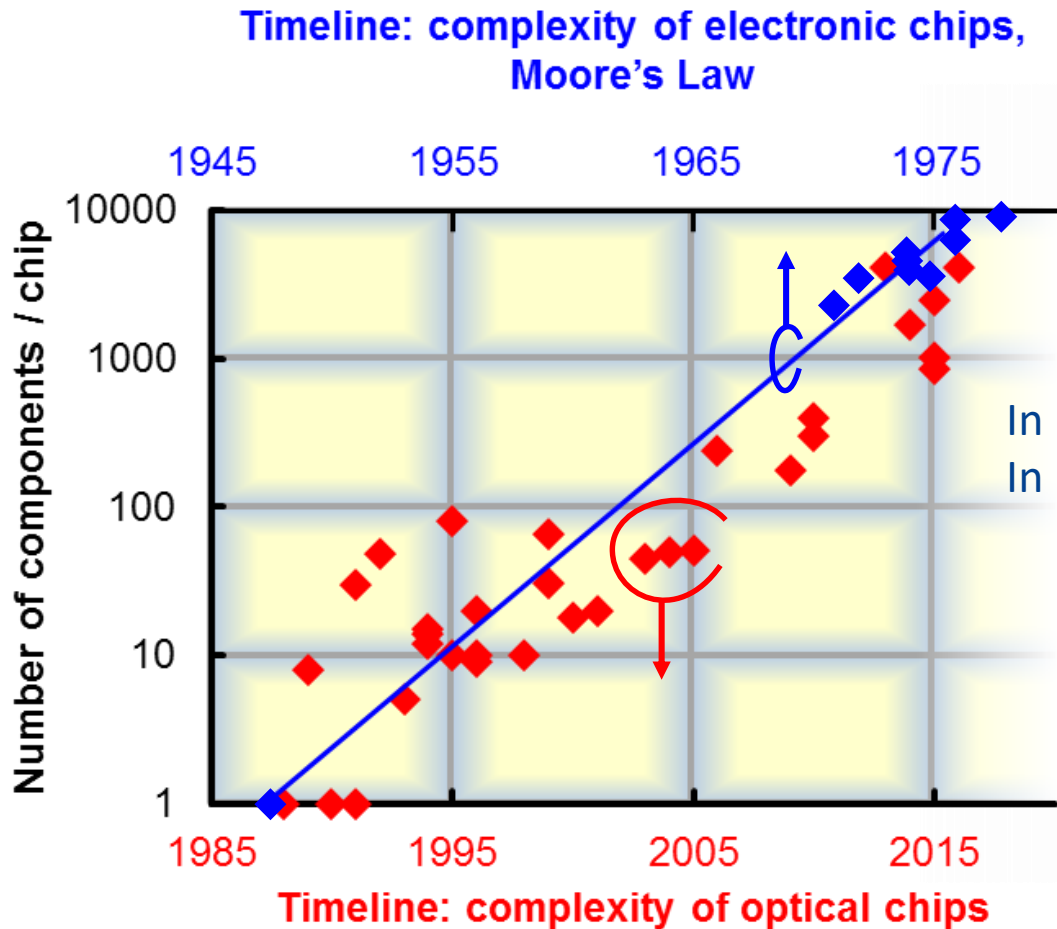


# Photonic integration: optical chips





# The number of components on an optical chip doubles every two years: Smit's Law



*exponential growth of*

- *bandwidth;*
- *devices connected to internet;*
- *sensor networks...*

In 1975 Bill Gates founded Microsoft...  
In 1976 Steve Jobs founded Apple...

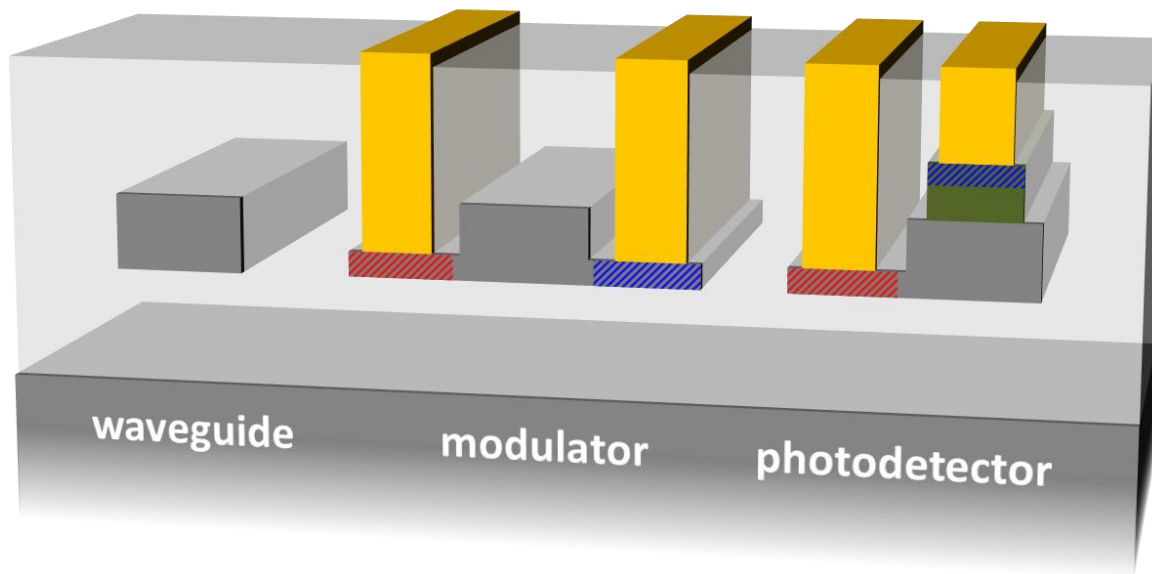
*technology drivers*

- *CMOS processes;*
- *open foundries;*
- *mature design software...*



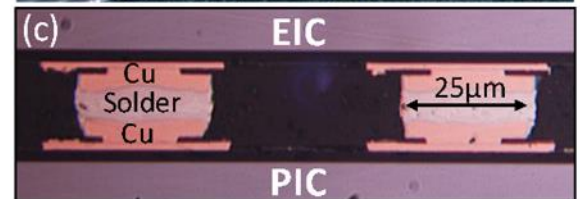
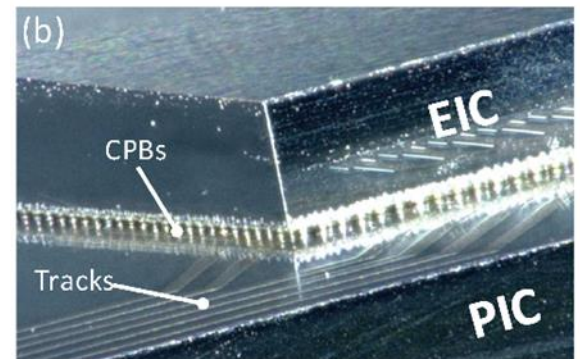
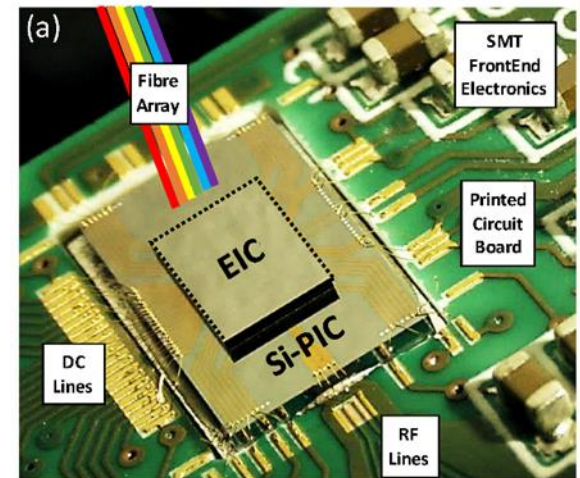
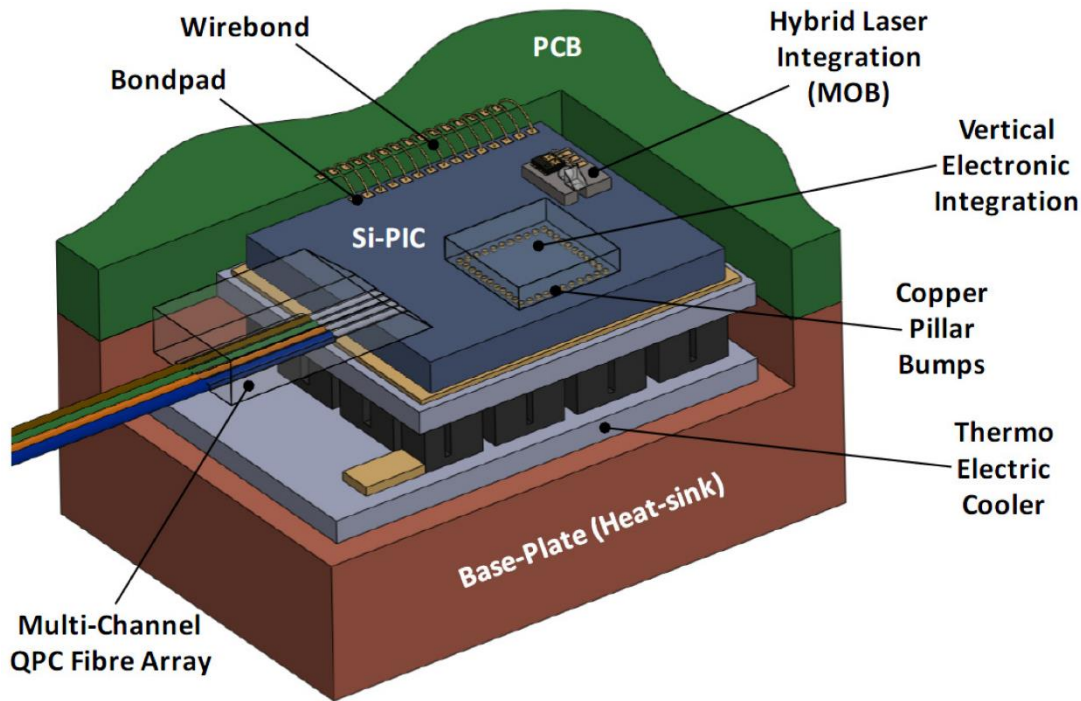
# Silicon photonics: CMOS compatible nanophotonics

- silicon
- silicon oxide
- germanium
- metal interconnect
- n-doping
- p-doping



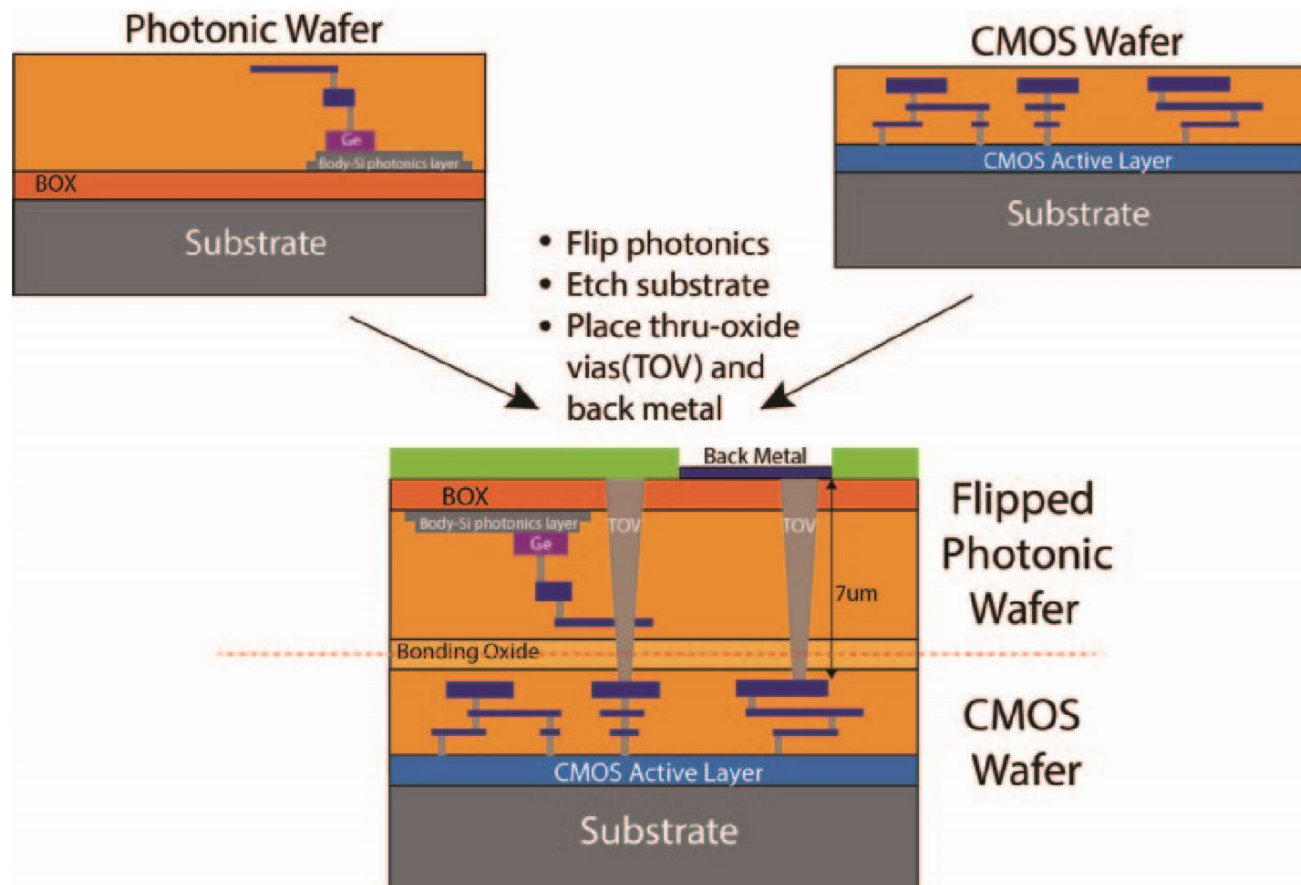
External laser  
typically needed

# Electronic-photonic integration: copper pillar bump bonding



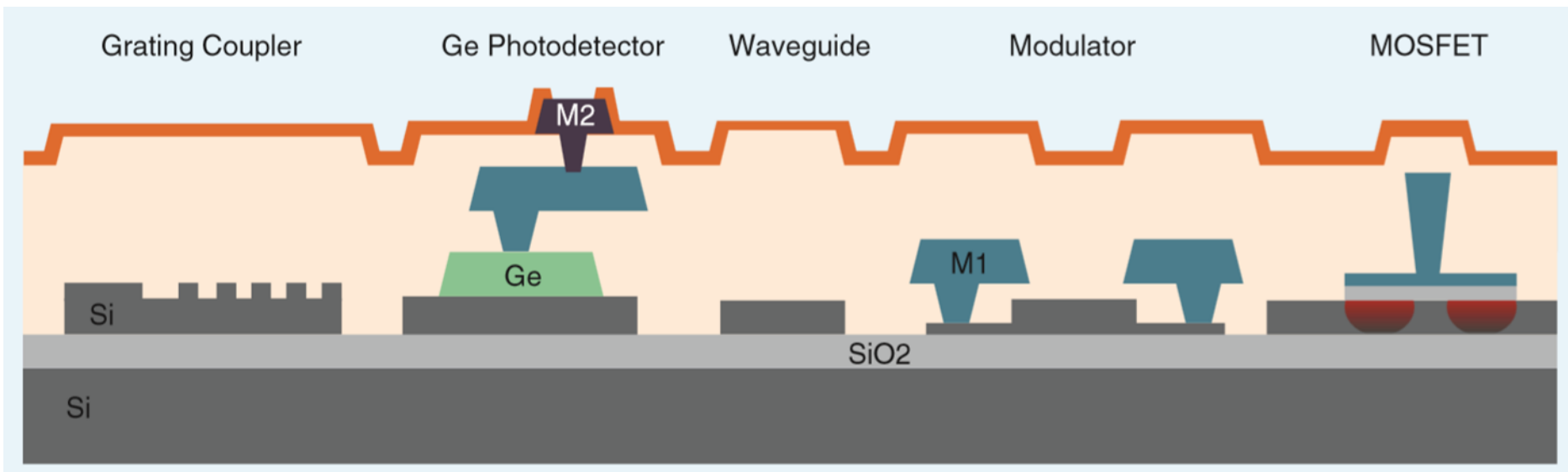
L. Carroll, *Appl. Sci.* 6, 12 (2016)

# Waferscale electronic-photonic integration: through-oxide vias



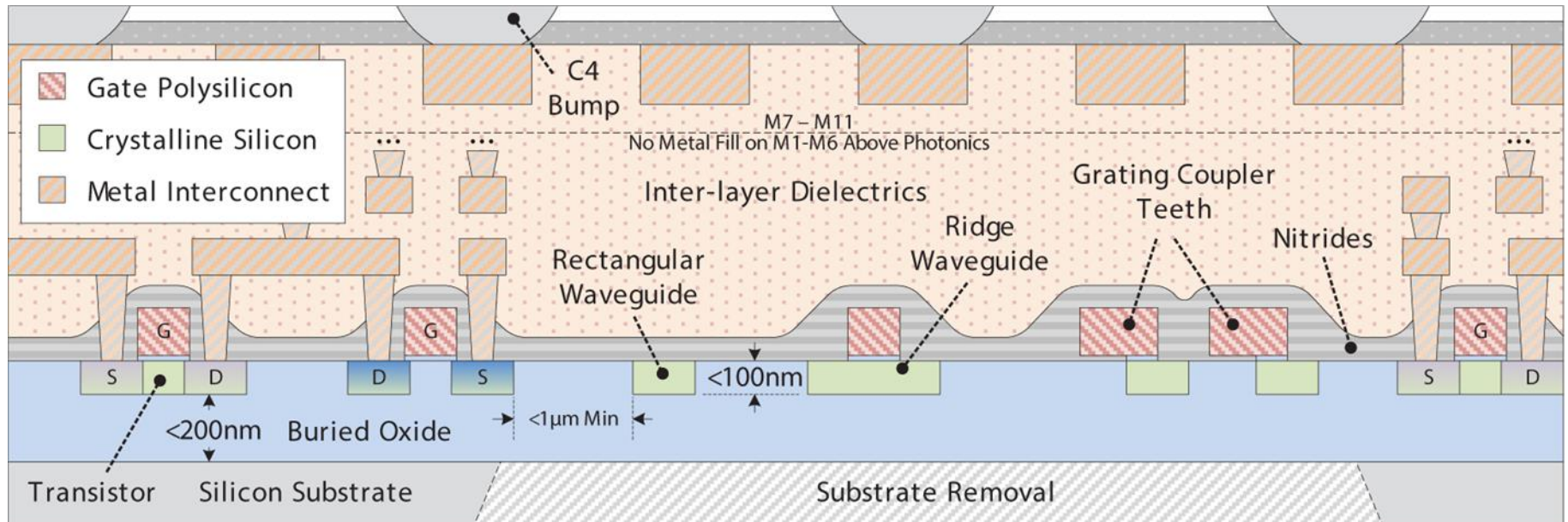
*N. DiLello Heidel, IEEE JSTQE, 22, 6 (2016)*

# Monolithic electronic-photonic integration: 130 nm / 90 nm dedicated CMOS processes



*Hochberg, IEEE Solid-State Circuits Magazine, Winter 2013*

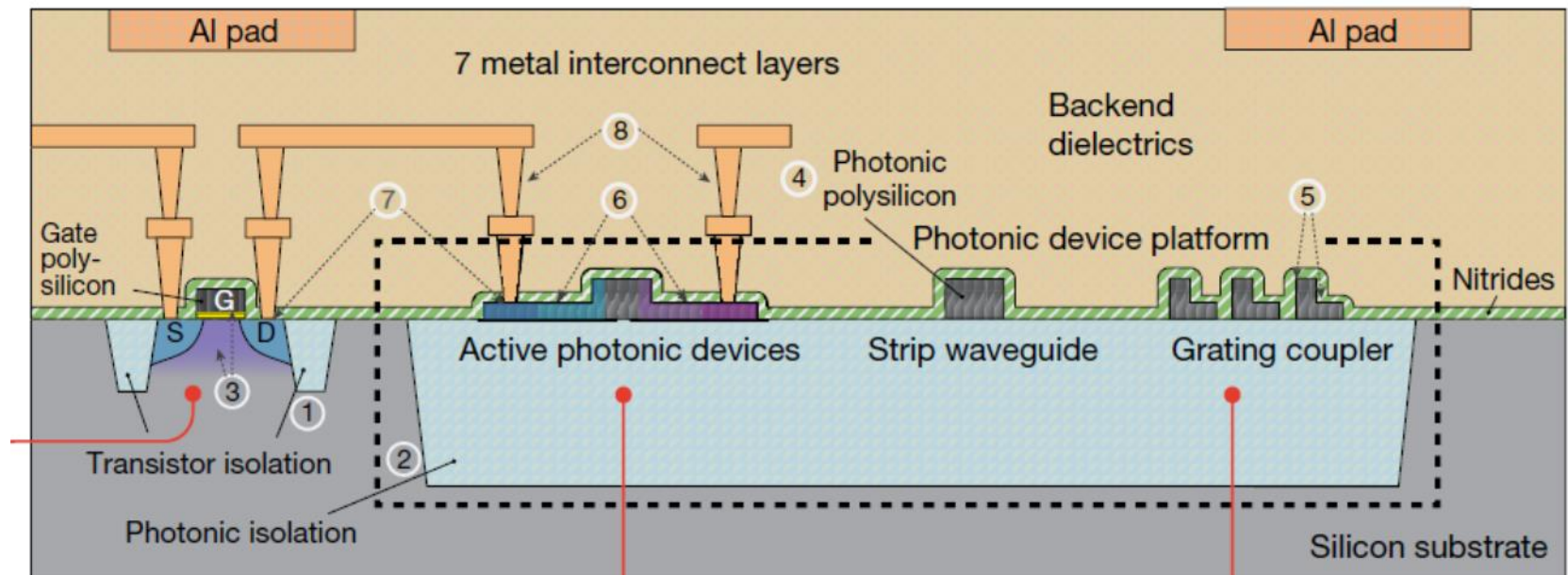
# Zero-change electronic-photonic integration: 45 nm / 32 nm CMOS processes



*Sun et al., JSSC. 50, 893 (2016)*



# Monolithic electronic-photonic integration: bulk CMOS process, 65-nm, 300-mm



*Atabaki et al., Nature 556, 7701 (2018)*

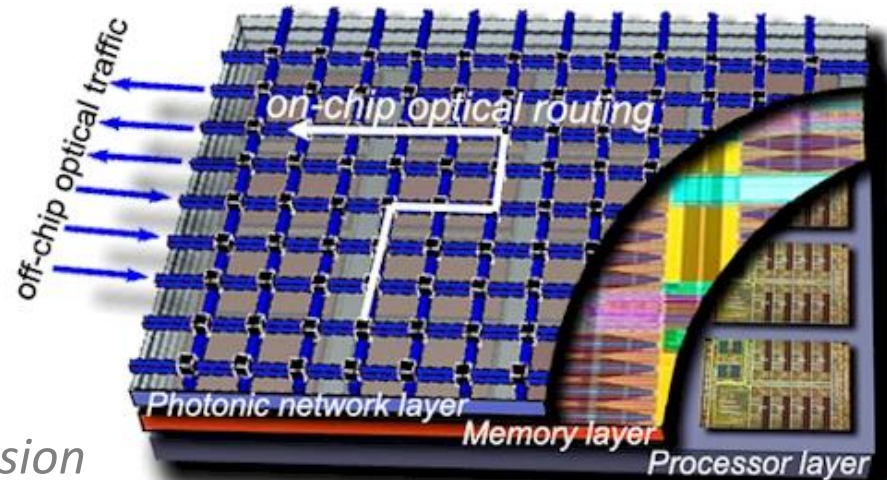
# STATUS OPTICAL NETWORKS ON CHIP?



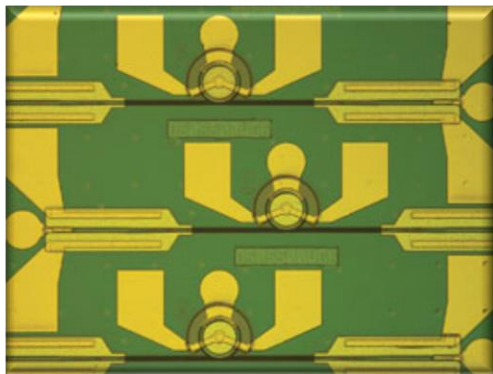


# Optical networks on chip: the future (?)

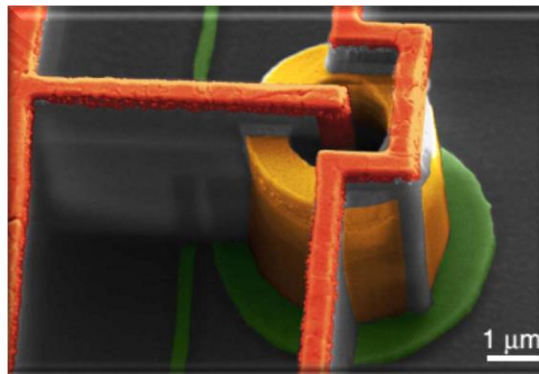
All components for an optical network in silicon have been realized by now



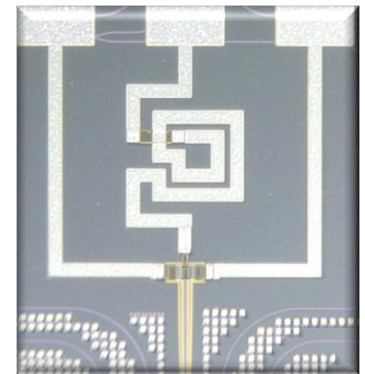
*IBM vision*



*lasers (UCSB)*



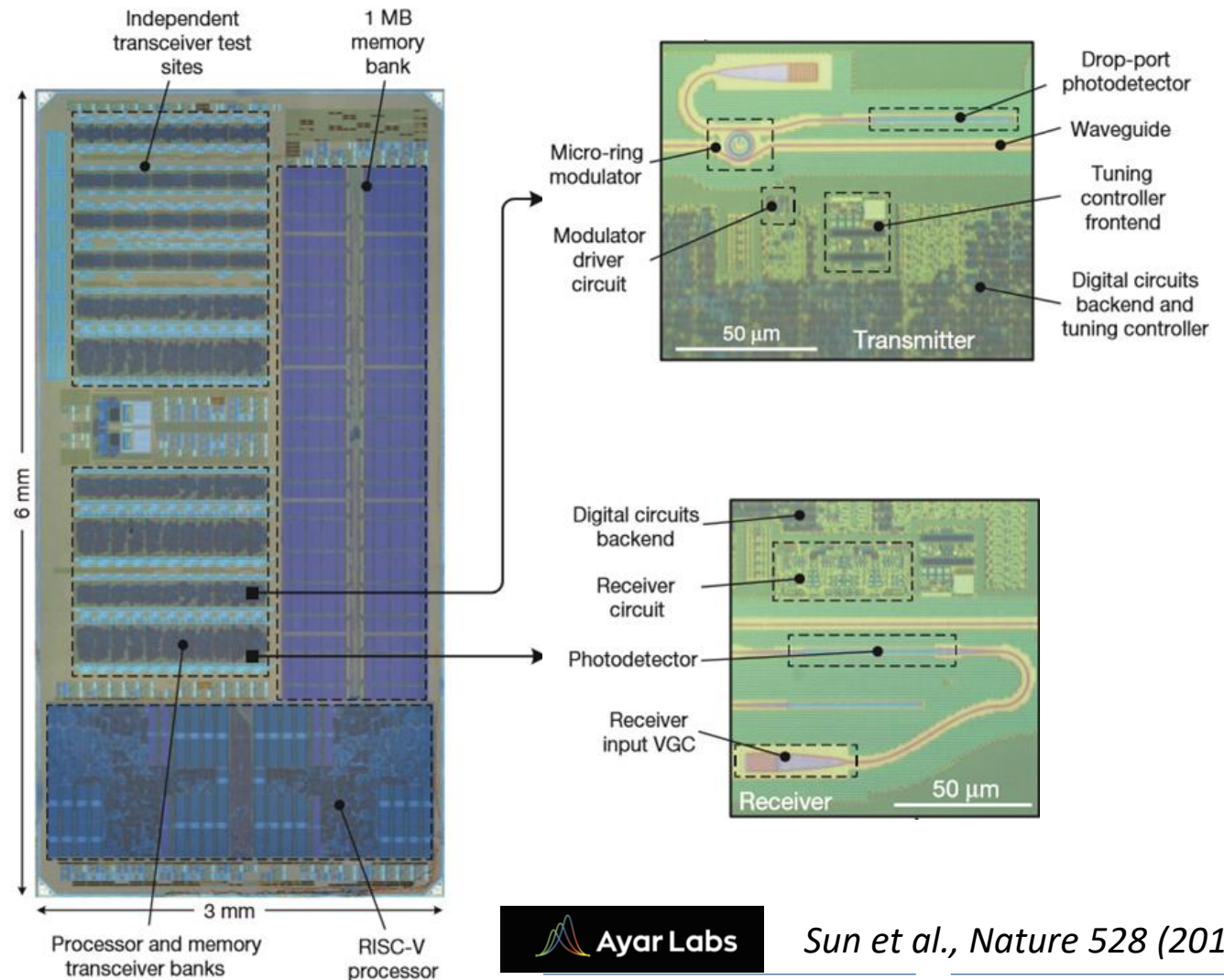
*modulator (MIT)*



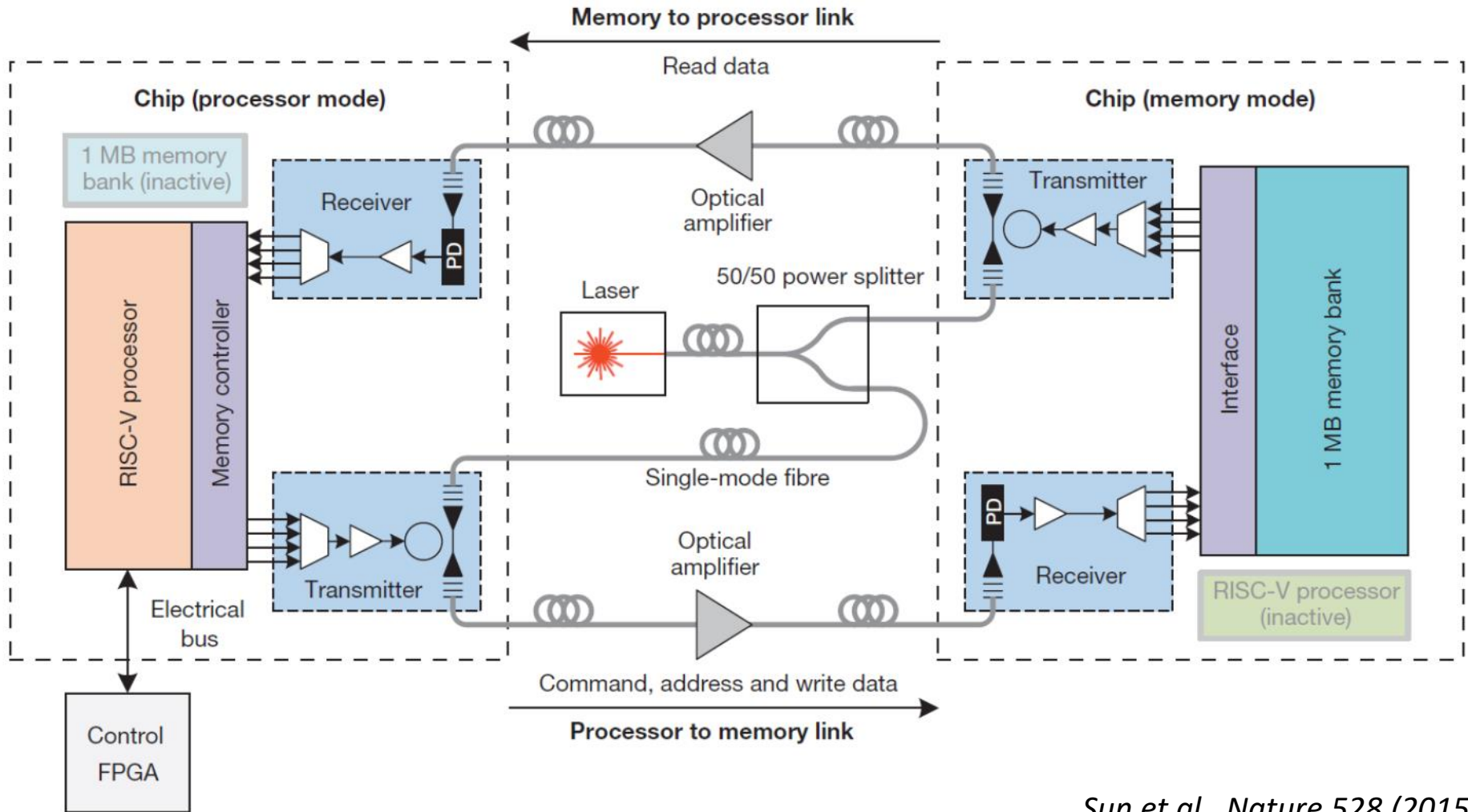
*detector (OP SIS)*

# Zero-change-process microprocessor with optical IO

70M transistors  
850 photonic components  
<200 nm BOX  
 $\lambda = 1180 \text{ nm}$   
5 Gbps per  $\lambda$

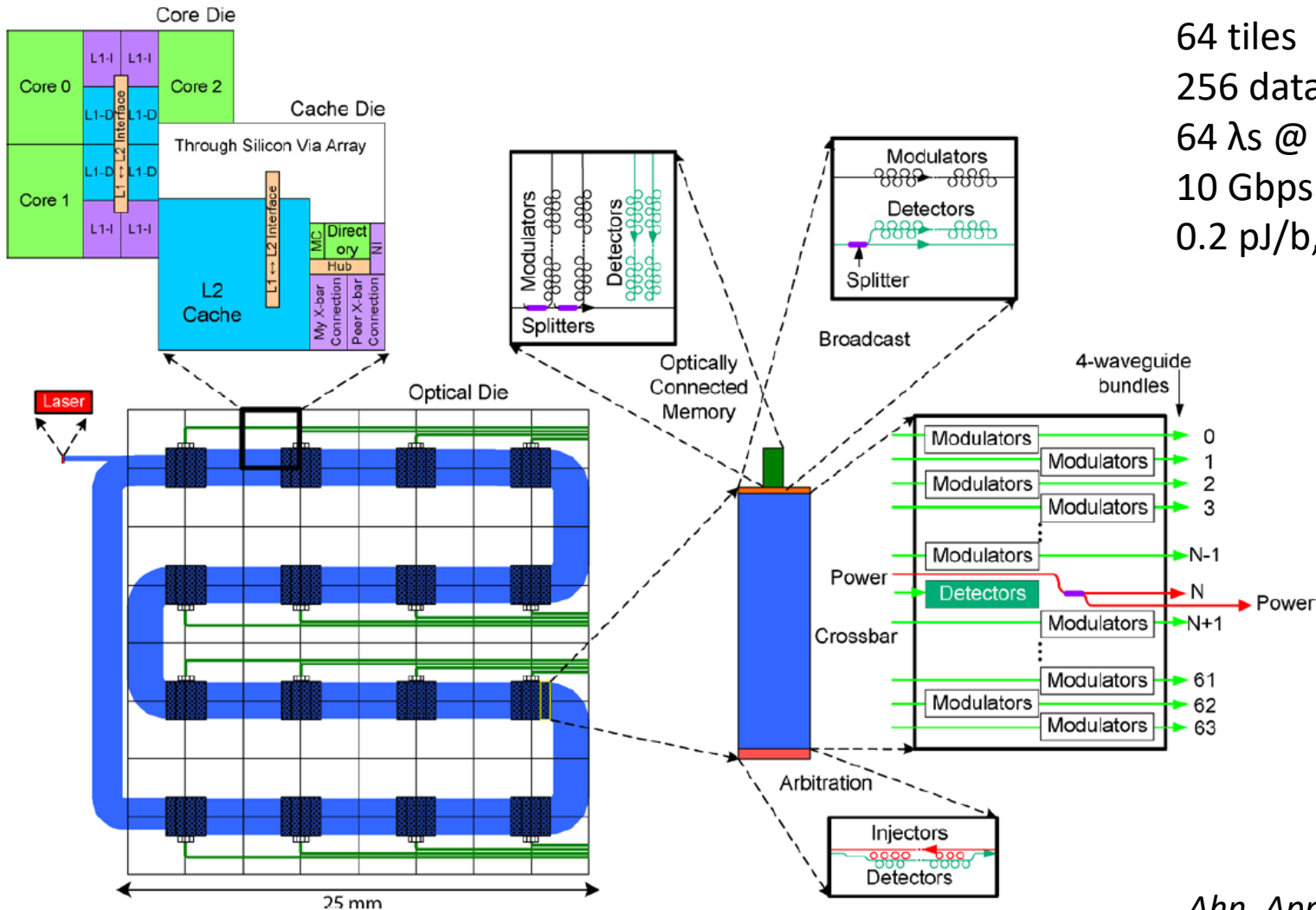


# Zero-change-process microprocessor with optical IO



*Sun et al., Nature 528 (2015)*

# HP's CORONA architecture

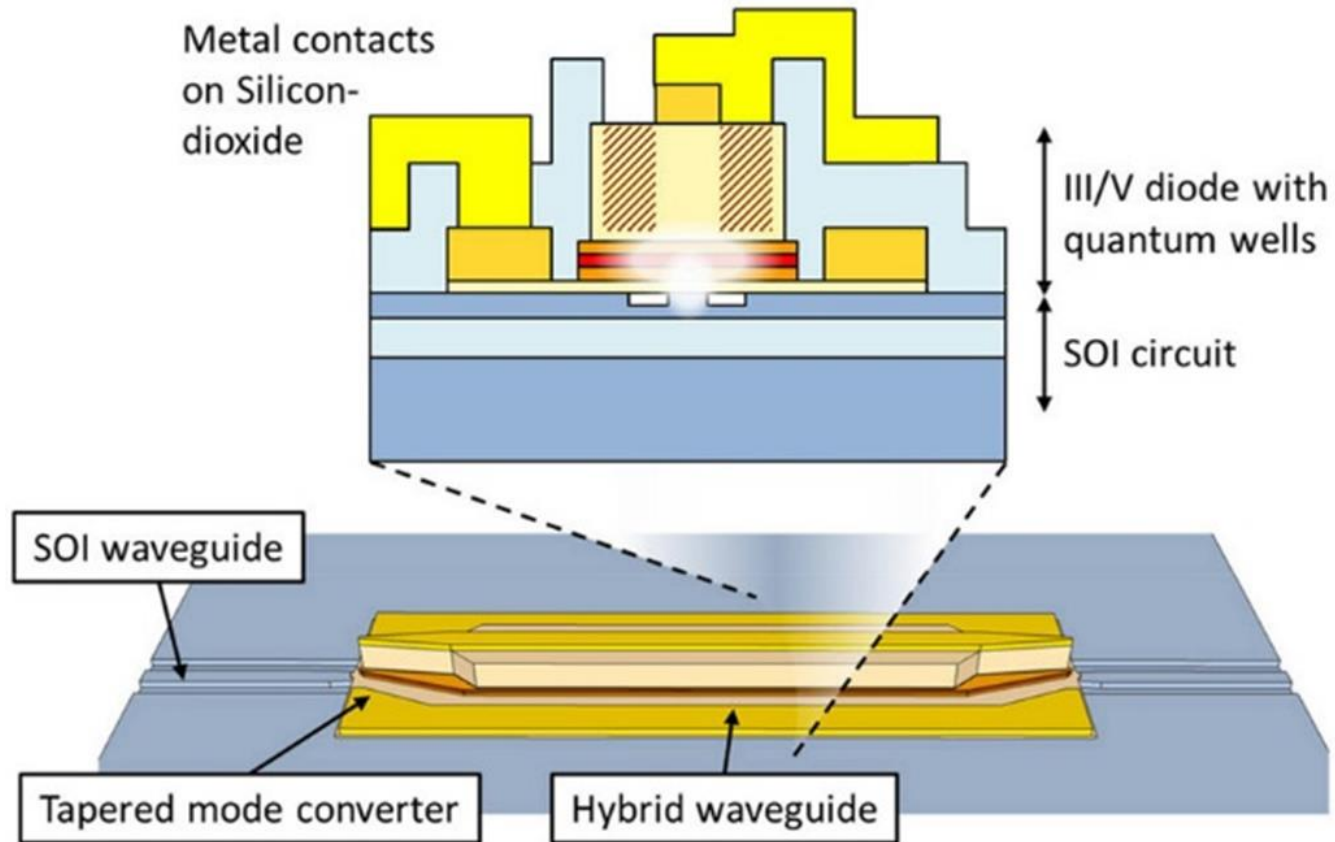


64 tiles  
 256 data/control wgs  
 64  $\lambda$ s @ 80 GHz  
 10 Gbps  $\rightarrow$  20 TBps  
 0.2 pJ/b, 40 W (17 nm)

*Ahn, Appl Phys A (2009) 95*



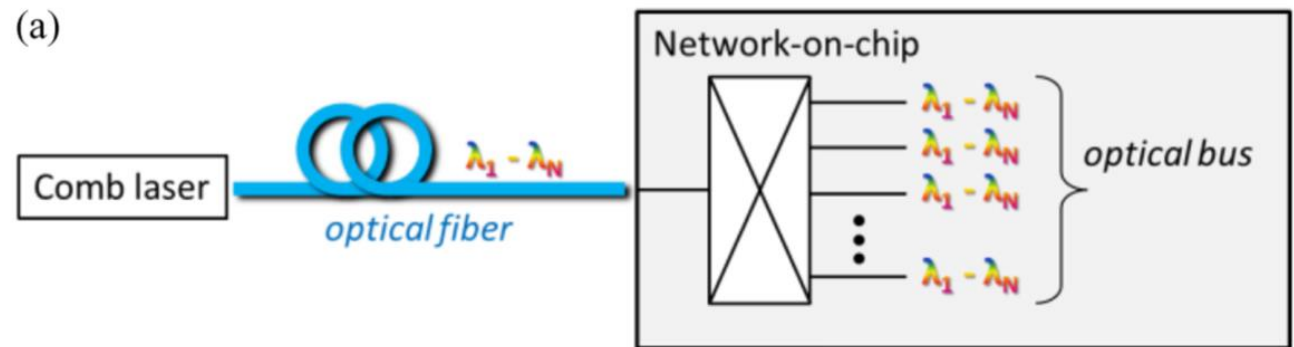
# On-chip lasers for energy efficiency and energy proportionality



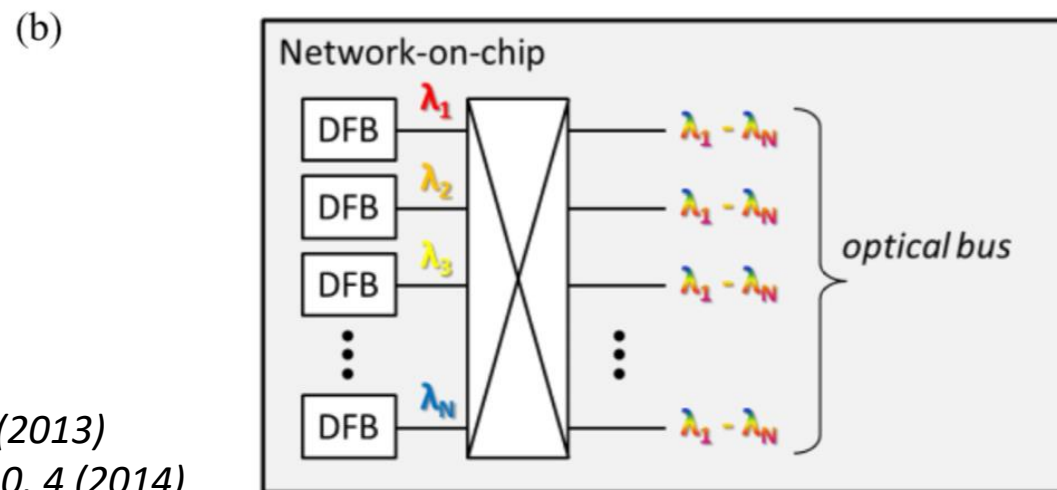
Heck et al., *IEEE JSTQE* 19, 4 (2013)  
Heck & Bowers, *IEEE JSTQE* 20, 4 (2014)



# On-chip lasers for energy efficiency and energy proportionality

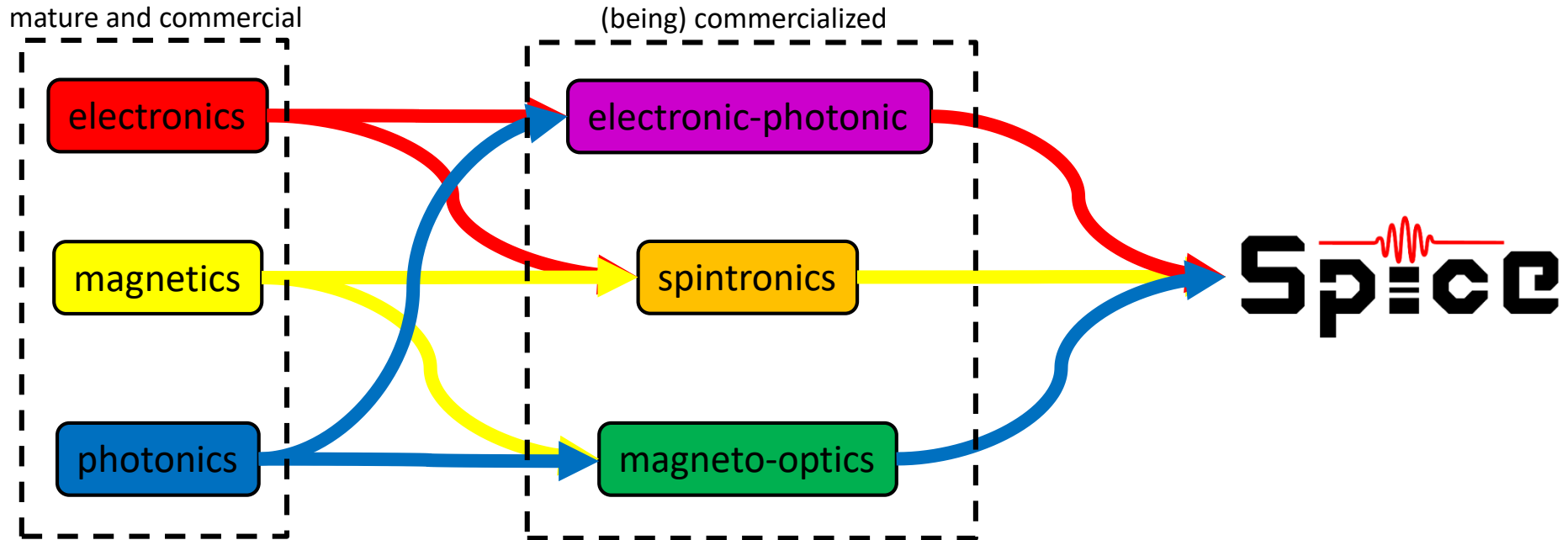


Up to 20 dB  
energy saving at  
lower utilization



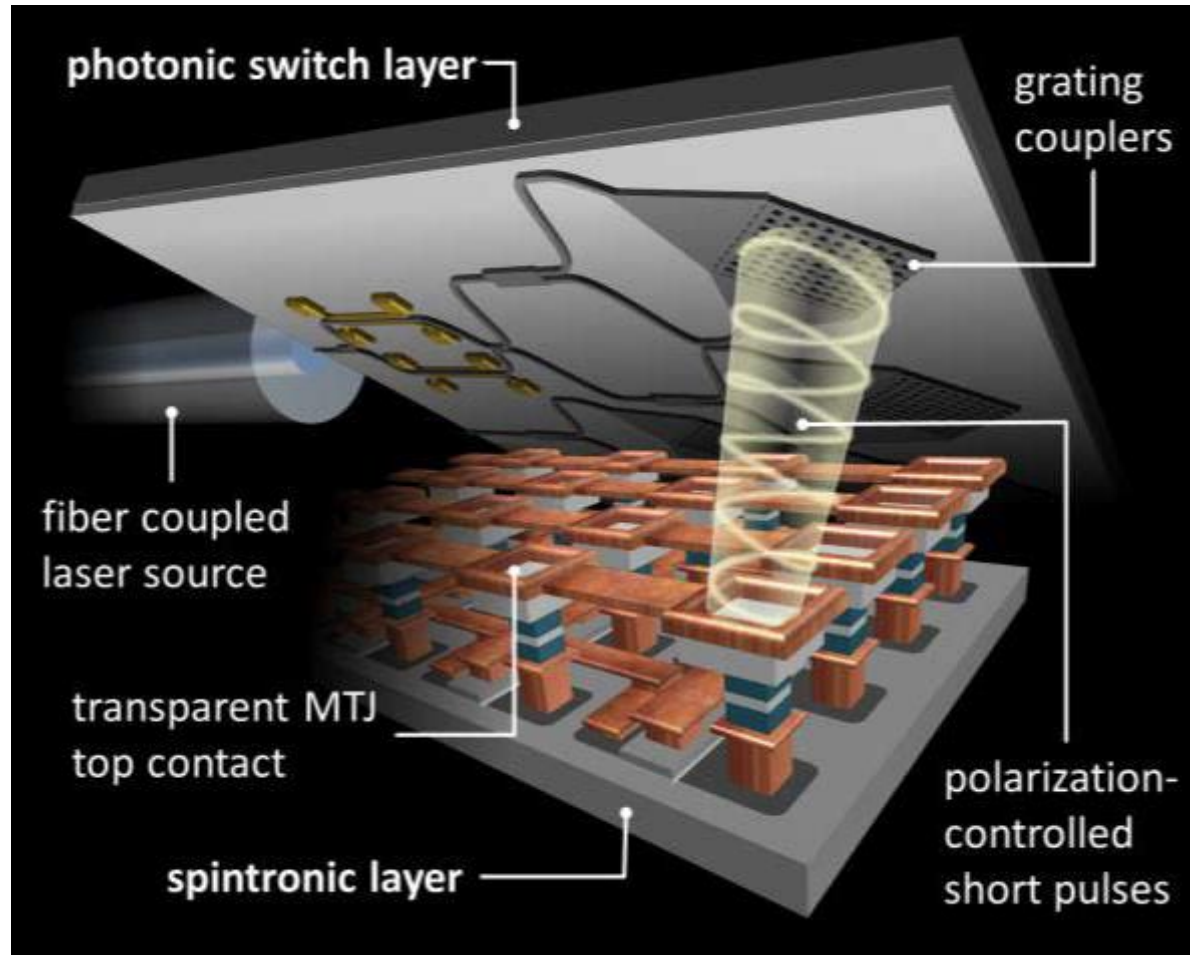
Heck et al., *IEEE JSTQE* 19, 4 (2013)  
Heck & Bowers, *IEEE JSTQE* 20, 4 (2014)

# Exponential technology trends converge



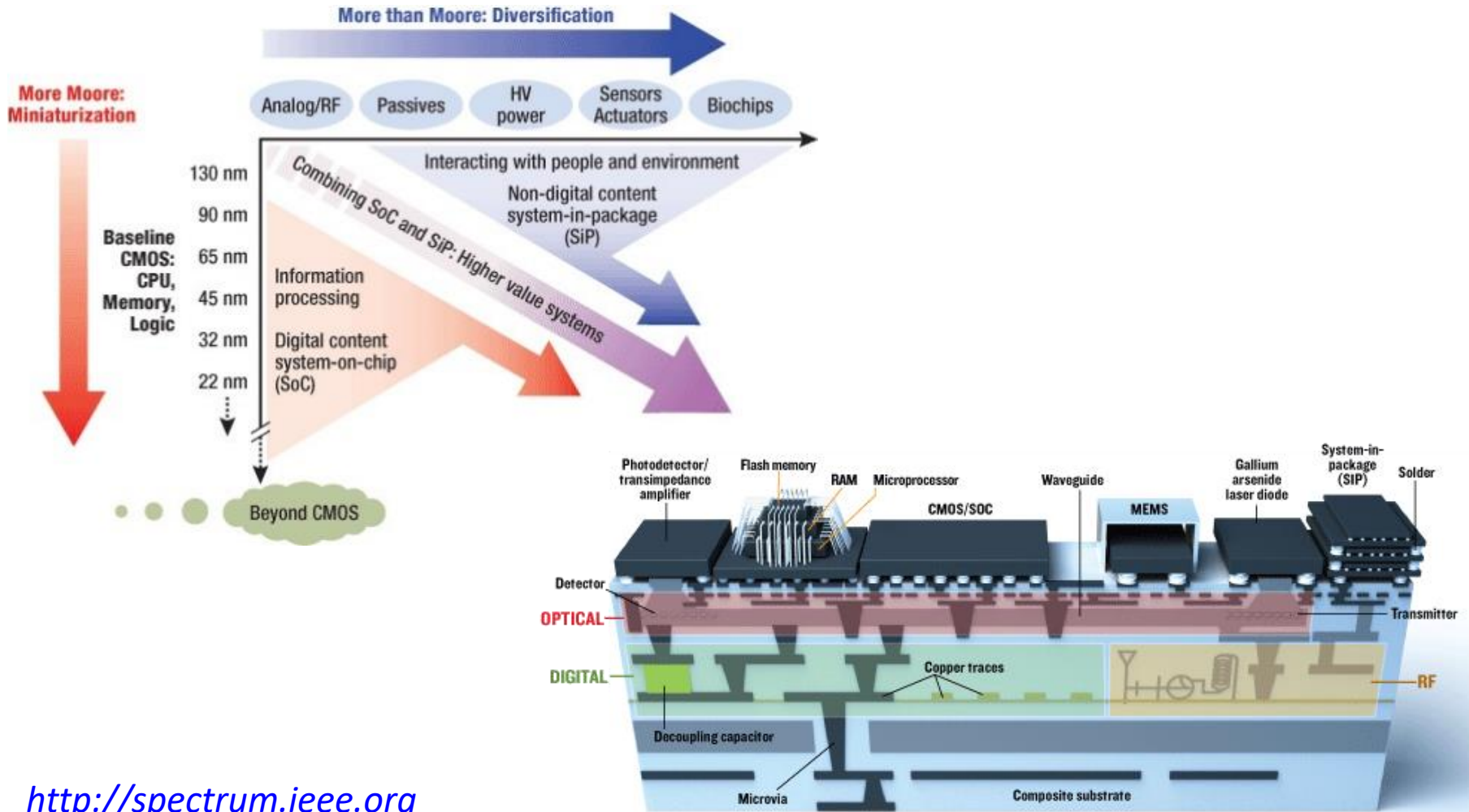


# Overall SPICE objective: spintronic-photonic integration platform



<http://spice-fetopen.eu/>

# More than Moore: SPICE technology for sensors and RF



<http://spectrum.ieee.org>



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