spintec
SPIN IN ELECTRONICS

Ultrafast *(+ high density)* MRAM strategies for cache applications and beyond

Lucian Prejbeanu

A. Timopheev, B. Lacoste, T. Devolder, M. Marins de Castro, U. Ebels, V. D. Nguyen, N. Perrissin, J. Chatterjee, L. Tillie, P. Coelho, S. Lequeux, G. Grégoire, Ph. Sabon, S. Auffret, E. Gautier, L. Buda-Prejbeanu, L. Vila, R. Sousa and B. Dieny

SPICE
SPIN PHENOMENA
INTERDISCIPLINARY CENTER

cea cnrs UNIVERSITÉ Grenoble Alpes Grenoble INP

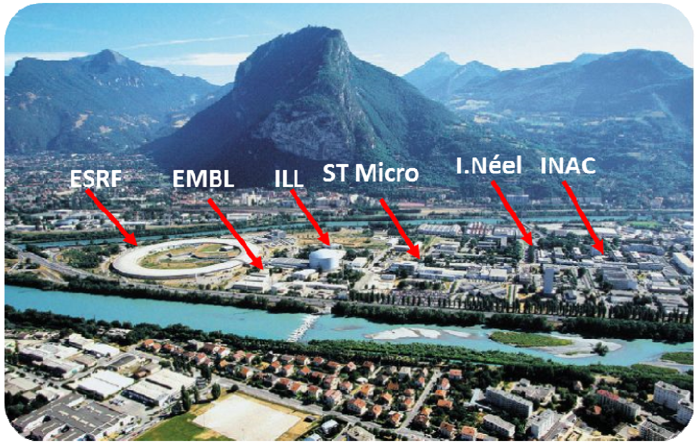
ULTRAFAST SPINTRONICS
FROM FUNDAMENTALS TO TECHNOLOGY

Mainz, Germany, October 24 2018

Outline of the talk

- 1. About SPINTEC & MRAM@SPINTEC
- 2. MRAM in the memory hierachy
- 3. Precessional STT-RAM with perpendicular polarizer
- 4. Use of 2nd order anisotropy in perpendicular STT-RAM
- 5. High speed SOT-MRAM
- Summary

SPINTEC *in brief*

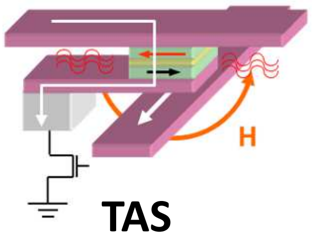


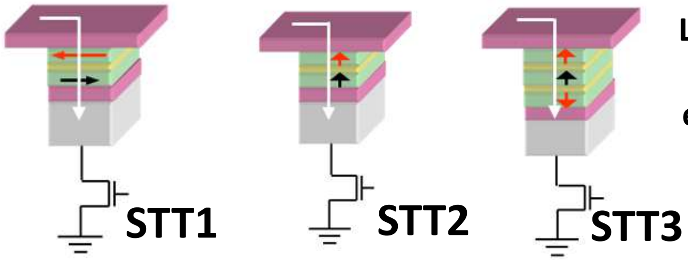
Created in 2002, now ~90-100 people

40 permanent people (30 researchers, 10 support)

50-60 PhDs , post-docs & visitors

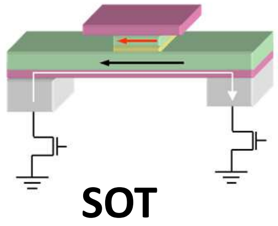
MRAM @ SPINTEC





Low-power hybrid electronics

Multifunctional hybrid electronics



NEXT

MOSAIC

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SPOT

GREAT

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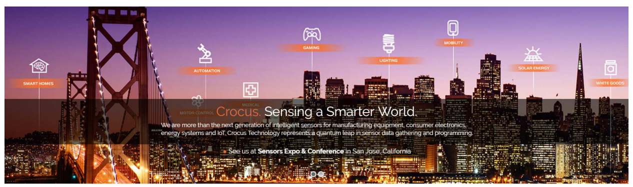
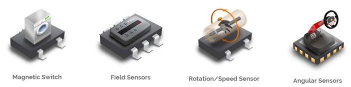
Spice

2002 2006 2010 2014 2015 2016 2017

CROCUS TECHNOLOGY
Intelligence in Sensing





eVaderis

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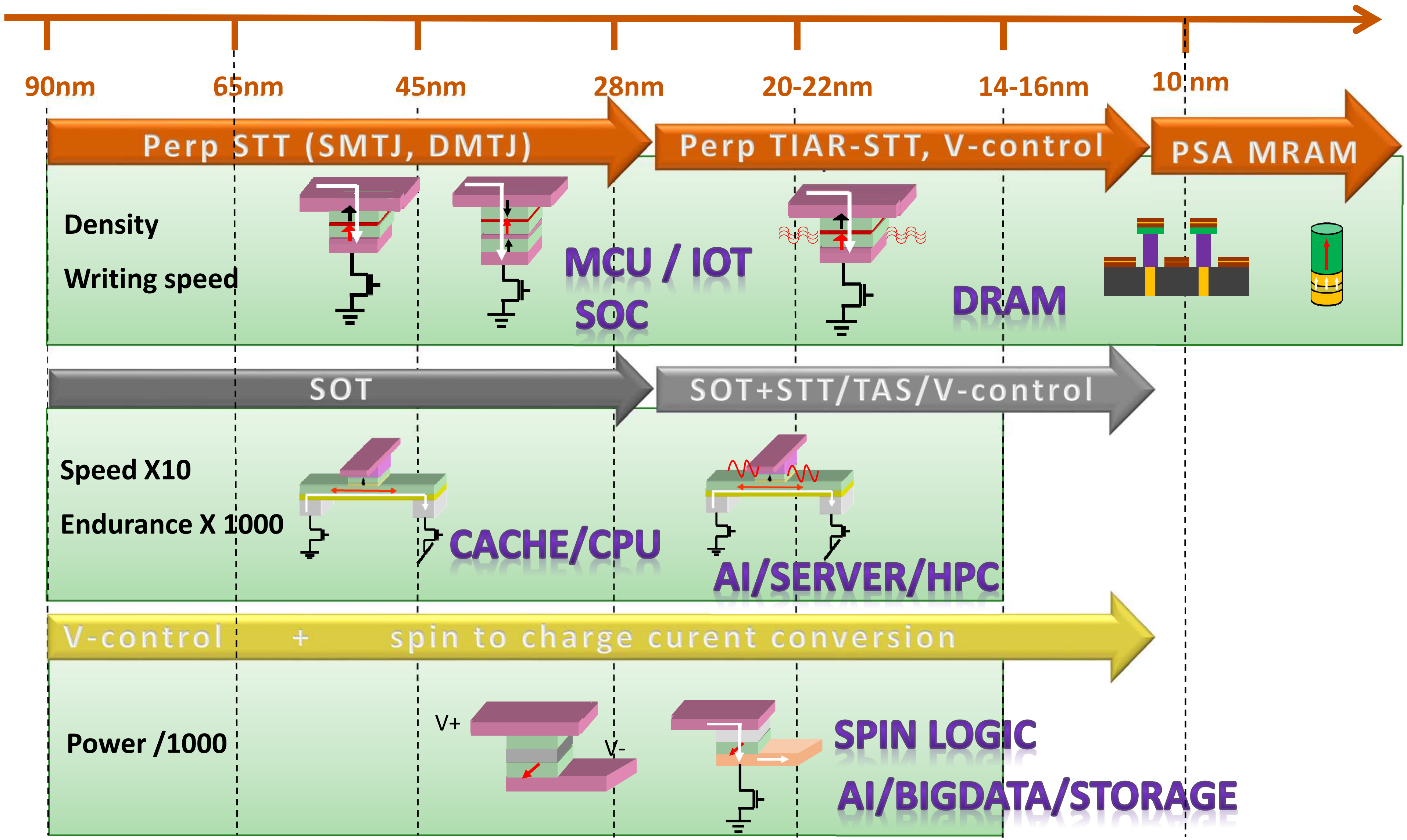
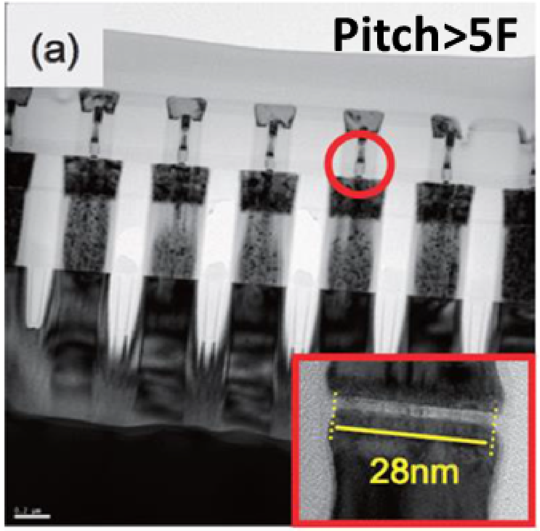
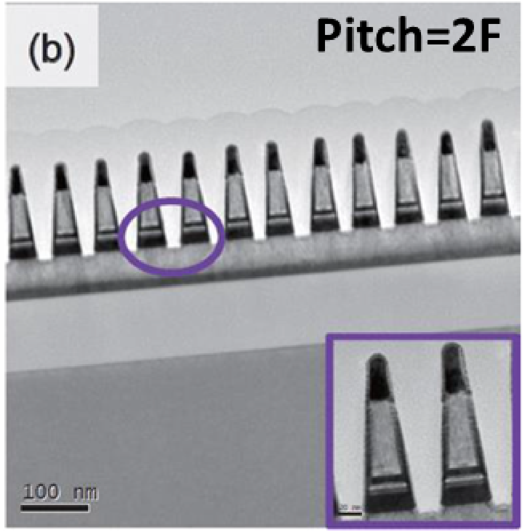
Spintronic – Application roadmap

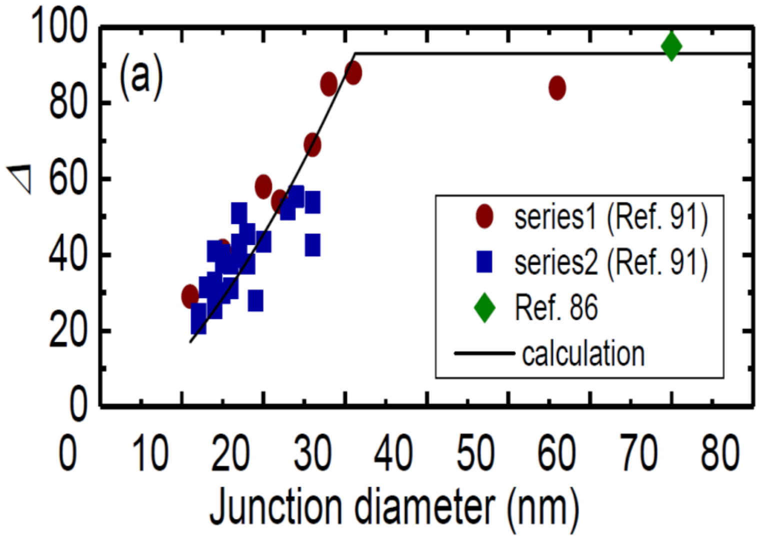


Nanopatterning of MTJ stacks
at very narrow pitch using IBE

Large decrease in thermal stability factor at sub-20 nm







Well patterned

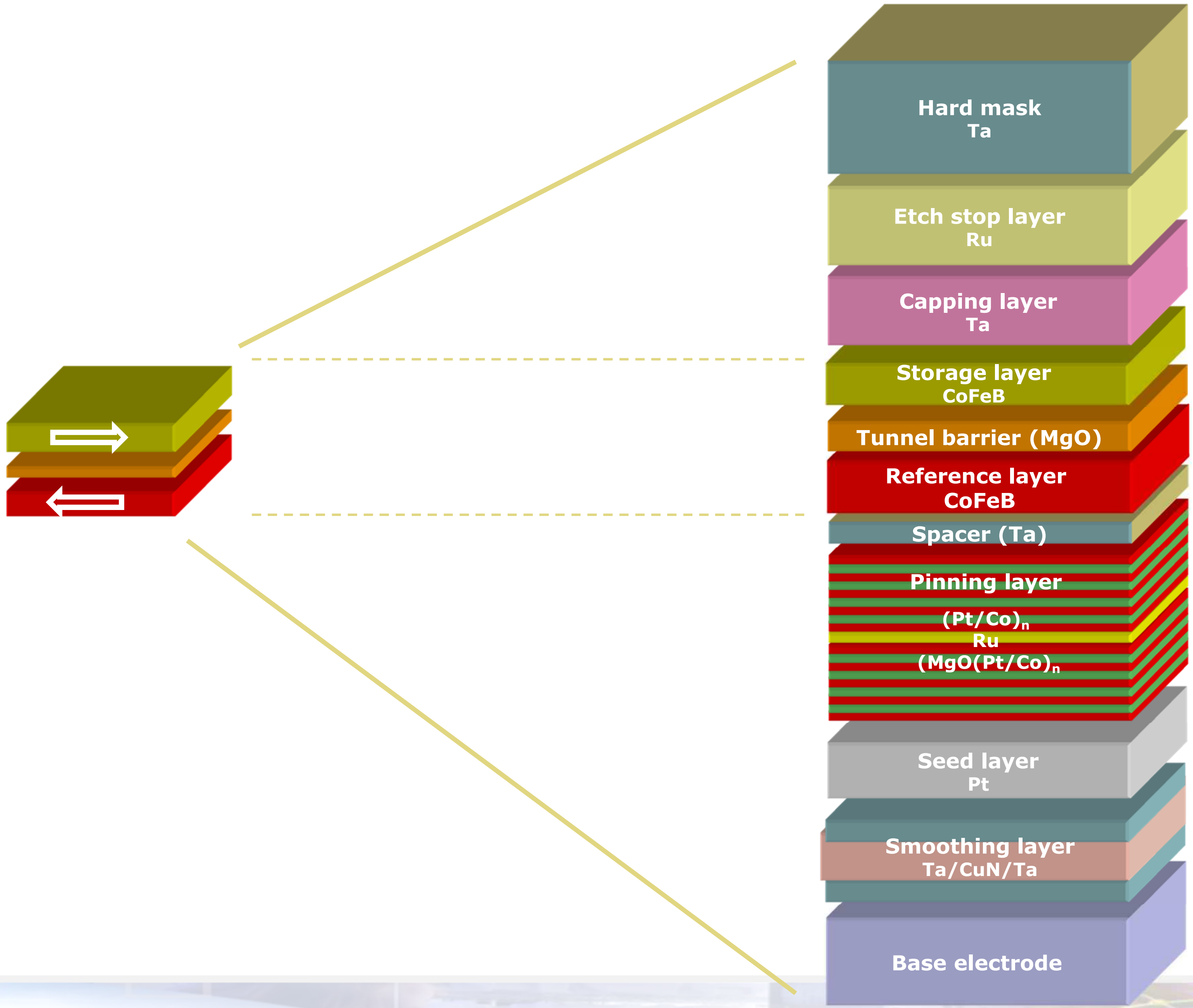
Shorts due to redeposition on sidewalls

Insufficient memory retention

Y. Kim et al, VLSI Symposium, pp. 210-211 (2011)
V. Ip et al, IEEE Trans. Mag. ***53,*** *2400104 (2017)*

L. Thomas et al, JAP ***115****, 172615 (2014)*
H. Sato et al, JJAP ***56****, 0802A6 (2017)*

MRAM challenges



Recent progress on industrial side

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Samsung ready to mass produce MRAM chips using 28nm FD-SOI process

Yiling Lin, Taipei; Jessie Shen, DIGITIMES [Tuesday 26 September 2017]

Samsung Foundry will soon be ready to enter mass production of magnetoresistive random-access memory (MRAM) chips built using 28nm fully depleted silicon-on-insulator (FD-SOI) process technology, according to Korea media reports.

Samsung is reportedly teaming up with NXP and has completed the tape-out of its 28nm FD-SOI embedded MRAM, which will be first applied to NXP's new low-power i.MX-series solution targeted at automotive, multimedia and display panel applications.

In related news, Synopsys announced recently its Design Platform has been fully certified for use on Samsung Foundry's 28nm FD-SOI process technology. A PDK and a comprehensive reference flow, compatible with Synopsys' Lynx Design System, containing scripts, design methodologies and best practices is now available.

TSMC to start eMRAM production in 2018

Jun 08, 2017 **MRAM production**

According to reports, Taiwan Semiconductor Manufacturing Company (TSMC) is aiming to start producing embedded MRAM chips in 2018 using a 22 nm process. This will be initial "risk production" to gauge market reception.

GLOBALFOUNDRIES

EVERSPIN TECHNOLOGIES The MRAM Company

GF-Everspin 2X nm eMRAM with superior data retention - VLSI Symposium

GLOBALFOUNDRIES and Everspin continue to drive embedded MRAM (eMRAM) forward into the 22nm process node! Please see our technical paper presented this week at VLSI Symposium in Japan.

For the first time, we are unveiling eMRAM that can retain data through solder reflow at 260C and 10+ years at 125C, plus read/write with outstanding endurance at 125C.

This is a major breakthrough from GLOBALFOUNDRIES and Everspin that enables eMRAM to be used fo general purpose MCU's and Automotive SOCs.

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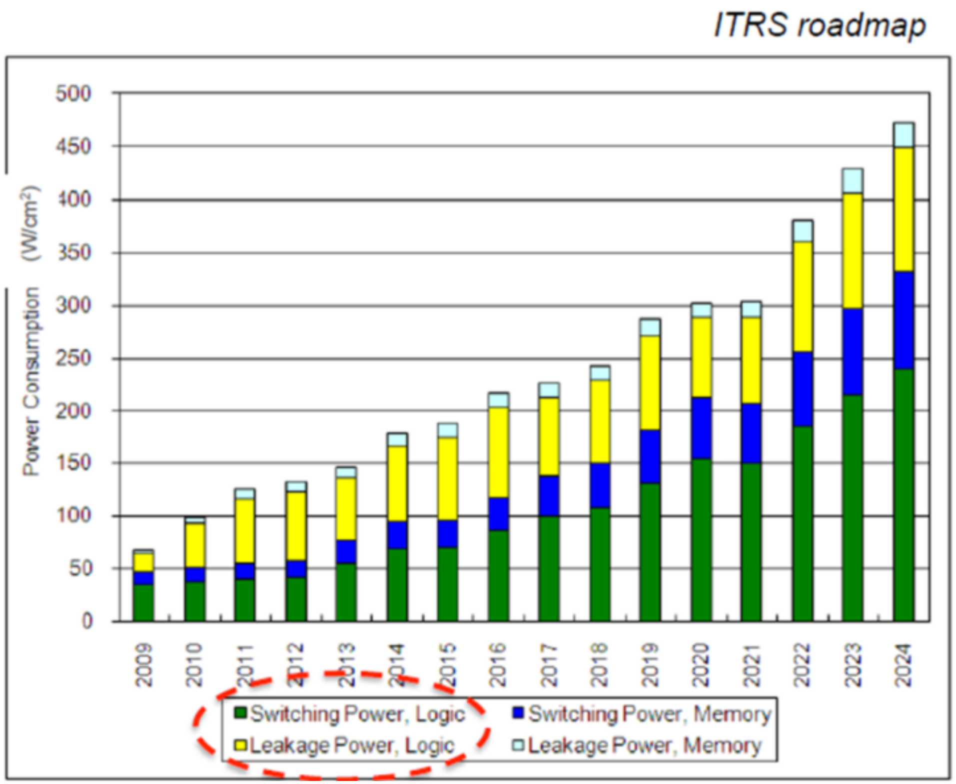
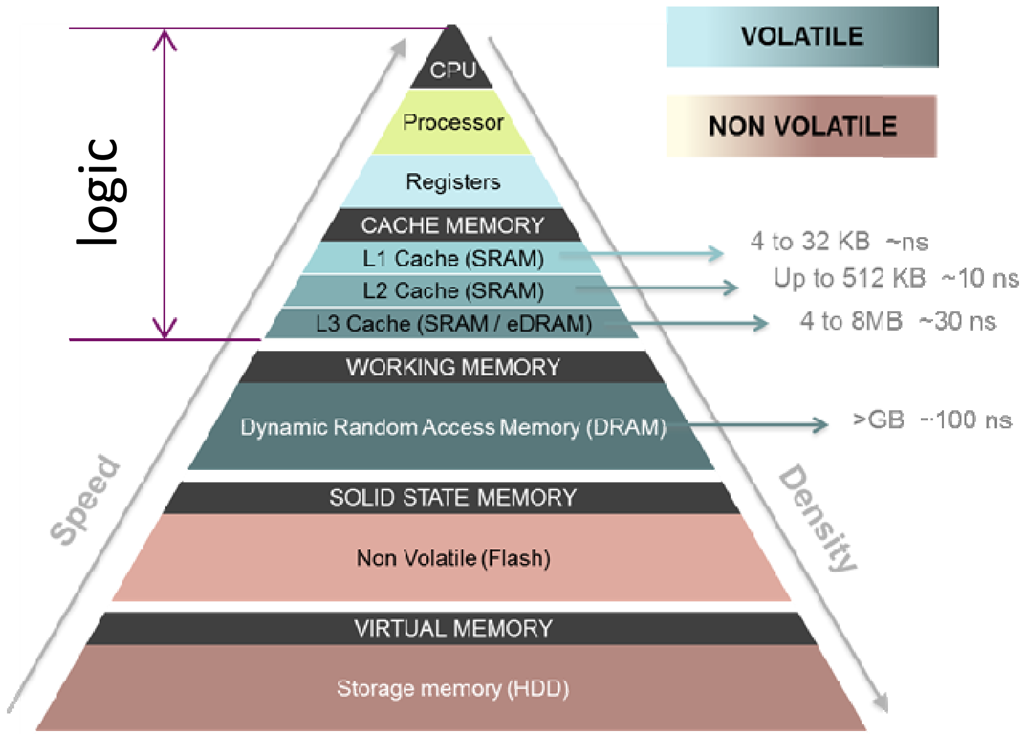
Memory hierarchy





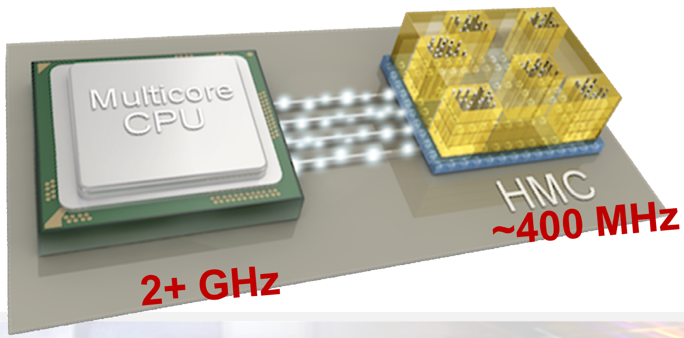
✓ **Bring non-volatility close to microprocessors**

✓ **Need for ultrafast memories (sub-ns) directly integrated (process, design) at the heart of the logic**

Memory vs. CPU speed mismatch

Logic keeps awaiting Data

Logic issue is becoming a memory issue !



How fast is fast enough?

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Density

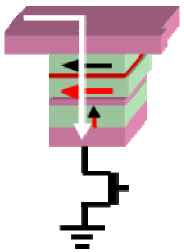
Storage disk drive TB ms	~100 MHz Main memory DRAM GB 3-20 ns	Cache SRAM kB – MB 0.5 - 2 ns	Registers	Processor 2 GHz

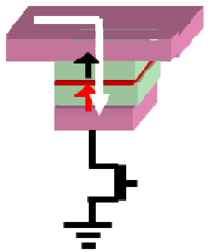
Speed

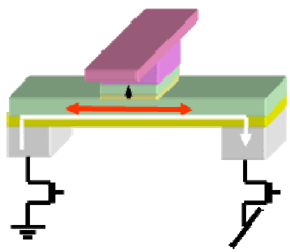
p-STT-RAM

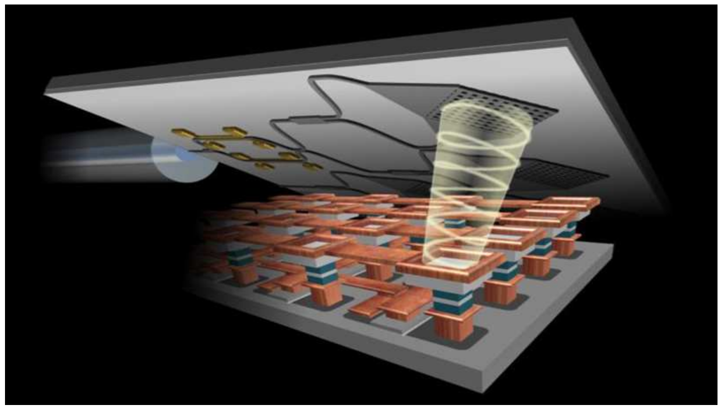
Need for a sub-ns switching MRAM

Spice









1 precesionnal

2 Easy cone

SPOT SOT

All optical switching

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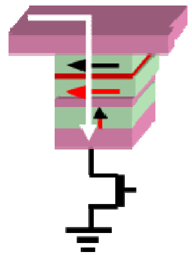


*Lacoste et al, PRB **89** (2014) 064408*
*Lacoste et al, PRB**90** (2014) 224404*

Latency + stochastic switching for STT-RAM

Polarization of spin-current aligned with magnetization equilibrium direction

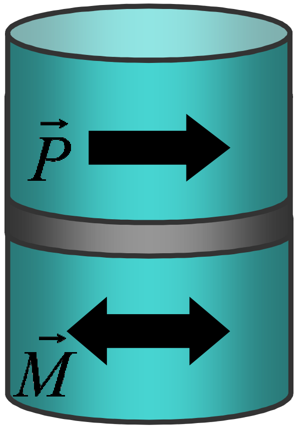
$$\frac{\partial \vec{M}}{\partial t}_{\mathrm{STT}} \propto V_{bias}(\vec{M} \times (\vec{P} \times \vec{M}))$$

In-plane

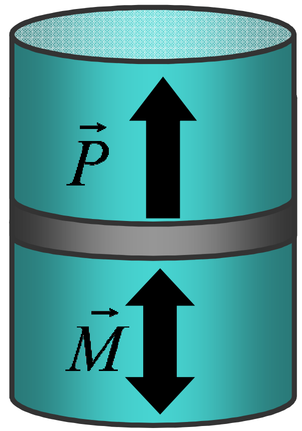
Reference

MgO

Storage



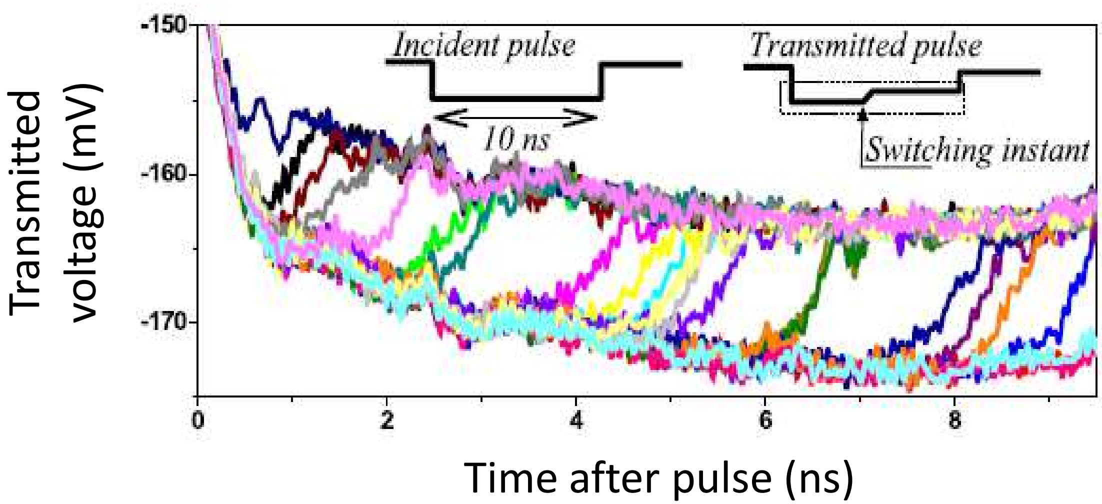
Out of plane



Stochastic reversal

Incubation time preceding a large thermal fluctuation

Reliable STTRAM writing requires more than a few ns



Devolder et al., Phys. Rev. Let. 100, 057206 (2006)

Devolder, Le Goff, Nikitin (SGMI Samsung collaboration) 2016

Solution: *perpendicular polarizer*

$$\mathrm{STT} \propto \eta_1(\vec{M} \times (\vec{P}_{\text{IN-PLANE}} \times \vec{M})) + \eta_2(\vec{M} \times (\vec{P}_{\text{OUT-OF-PLANE}} \times \vec{M}))$$

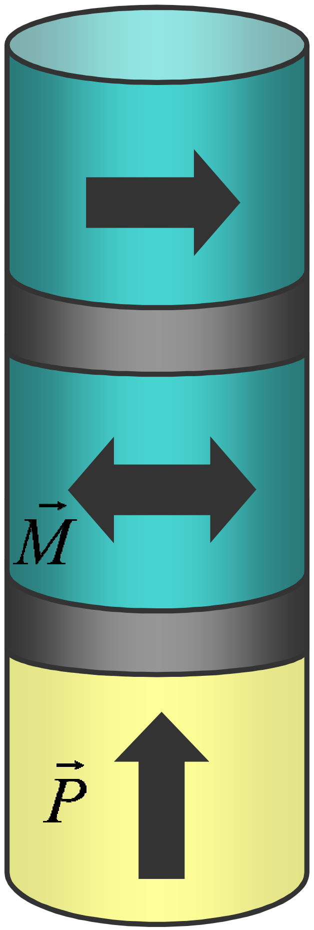
Reference Layer (Analyzer)

MgO

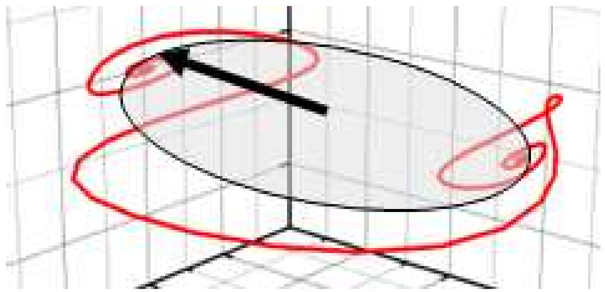
Free Layer

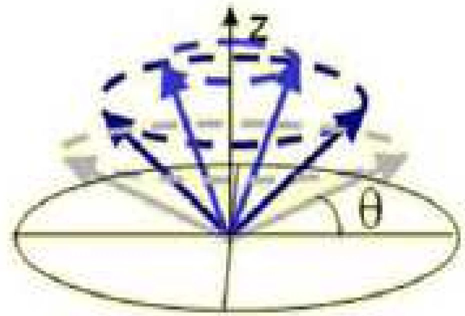
MgO (lower RA) or Cu

Perpendicular Polarizer



Patents Spintec FR0015893, US6532164B2





STT from in-plane analyzer:
Bipolar switching

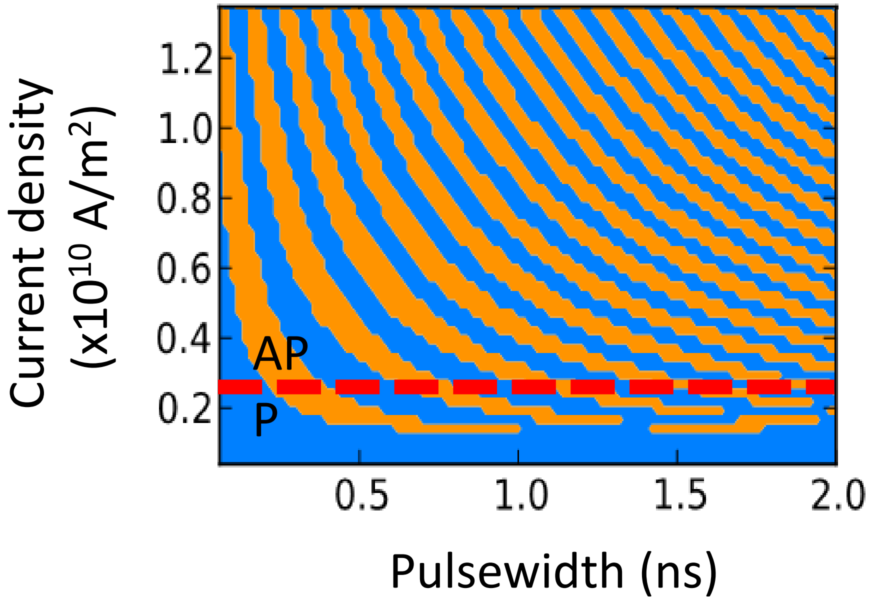
STT from Perpendicular polarizer:
Out-of-plane oscillations

How to conveniently tune the relative influence of these two STT contributions?

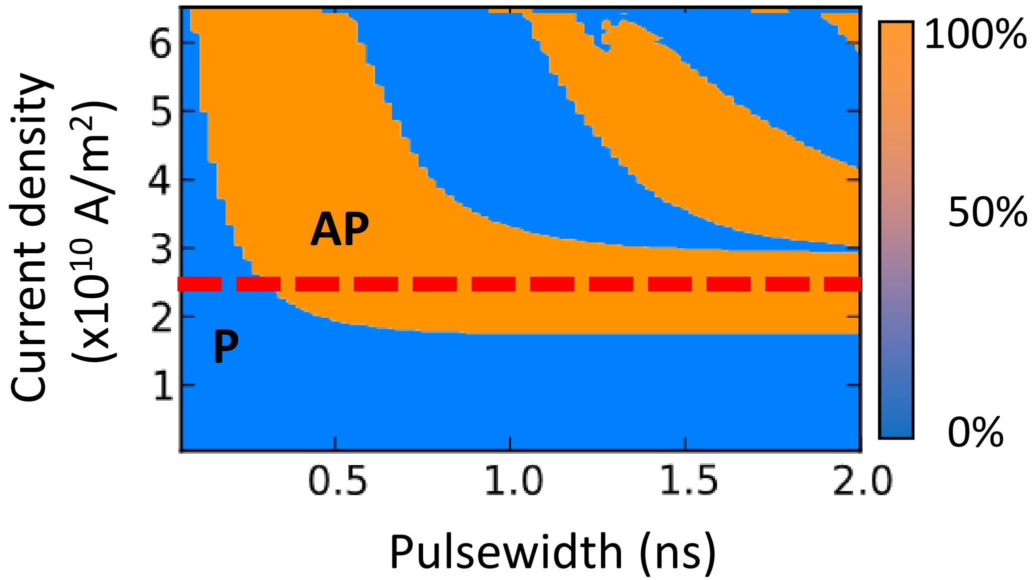
A: shape
B: transverse magnetic field

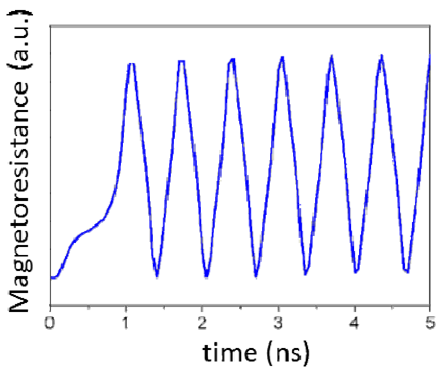
A: Influence of the shape (AR=2 vs AR=5)

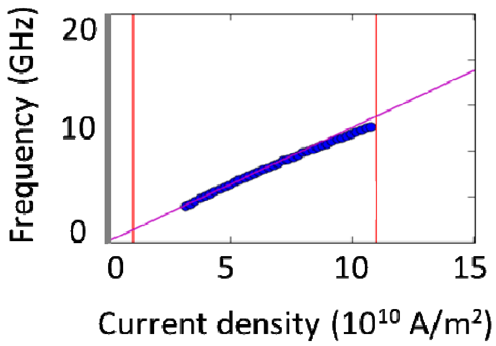
AR=2 Cell size : 80nm x 160nm



AR=5 Cell size : 50nm x 250nm







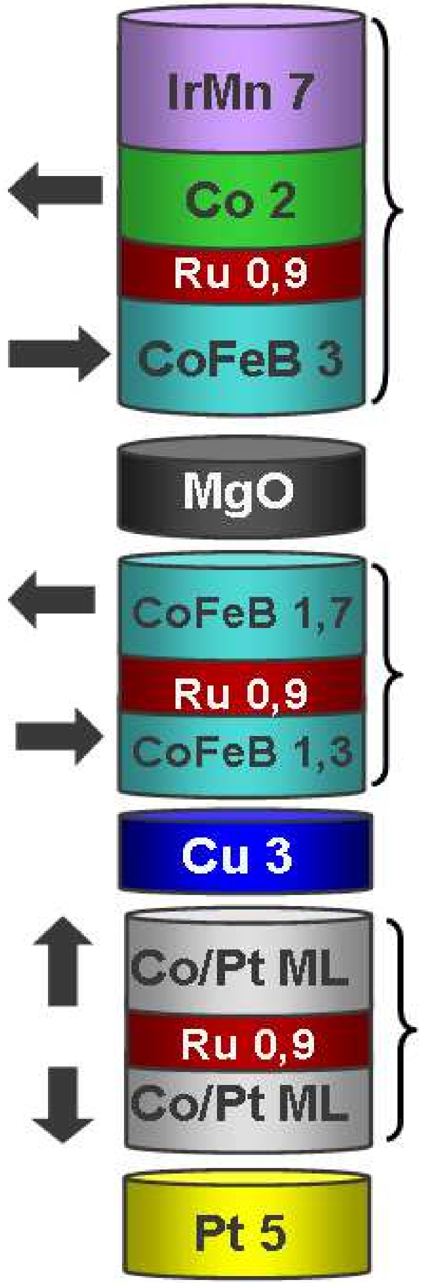
✓ Non-oscillatory bipolar switching can be achieved.

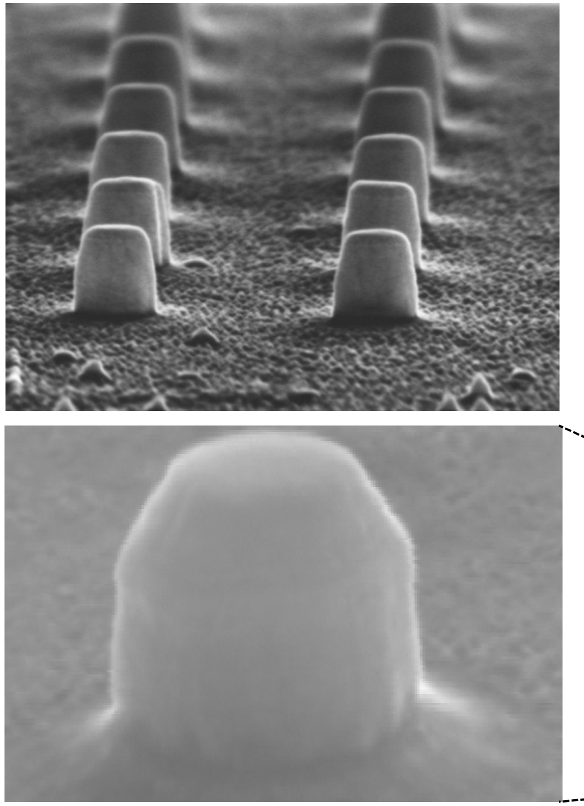
✓ Ultrafast reversal without incubation time

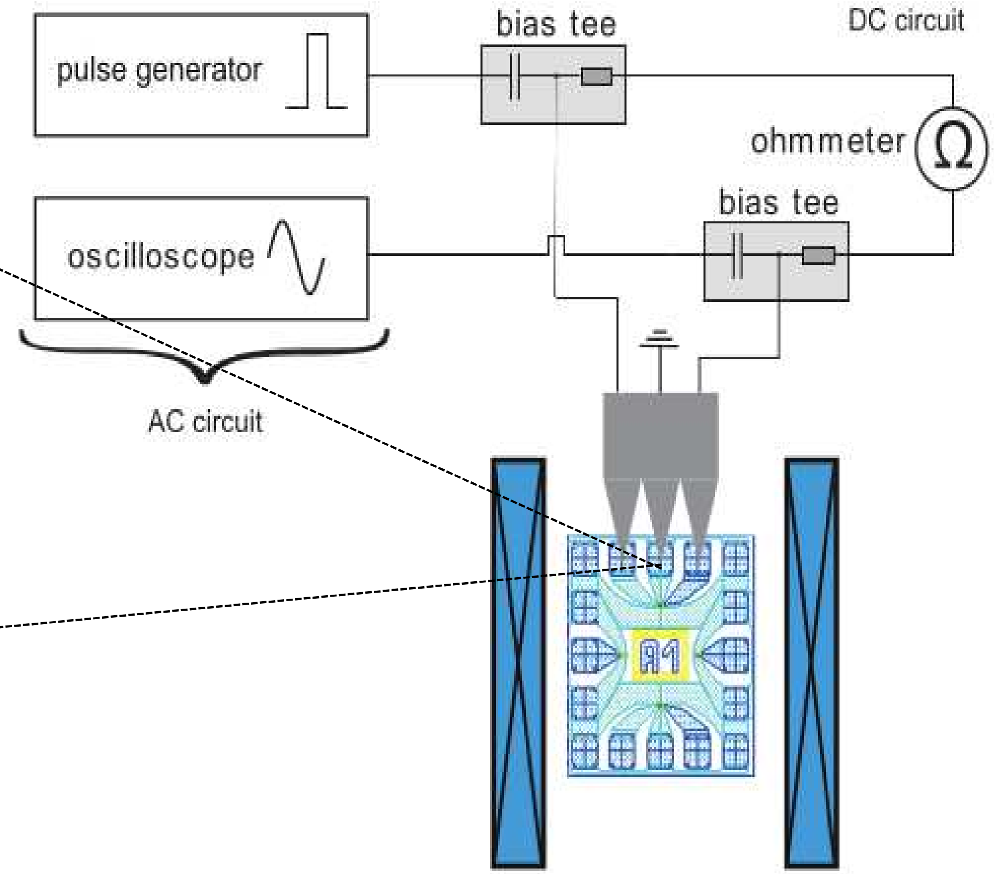
Out-of-plane precession of the free layer magnetization due to STT from perp polarizer

Macrospin simulations: B. Lacoste, L. Buda-Prejbeanu

Experimental evidence of the precessional STT-RAM

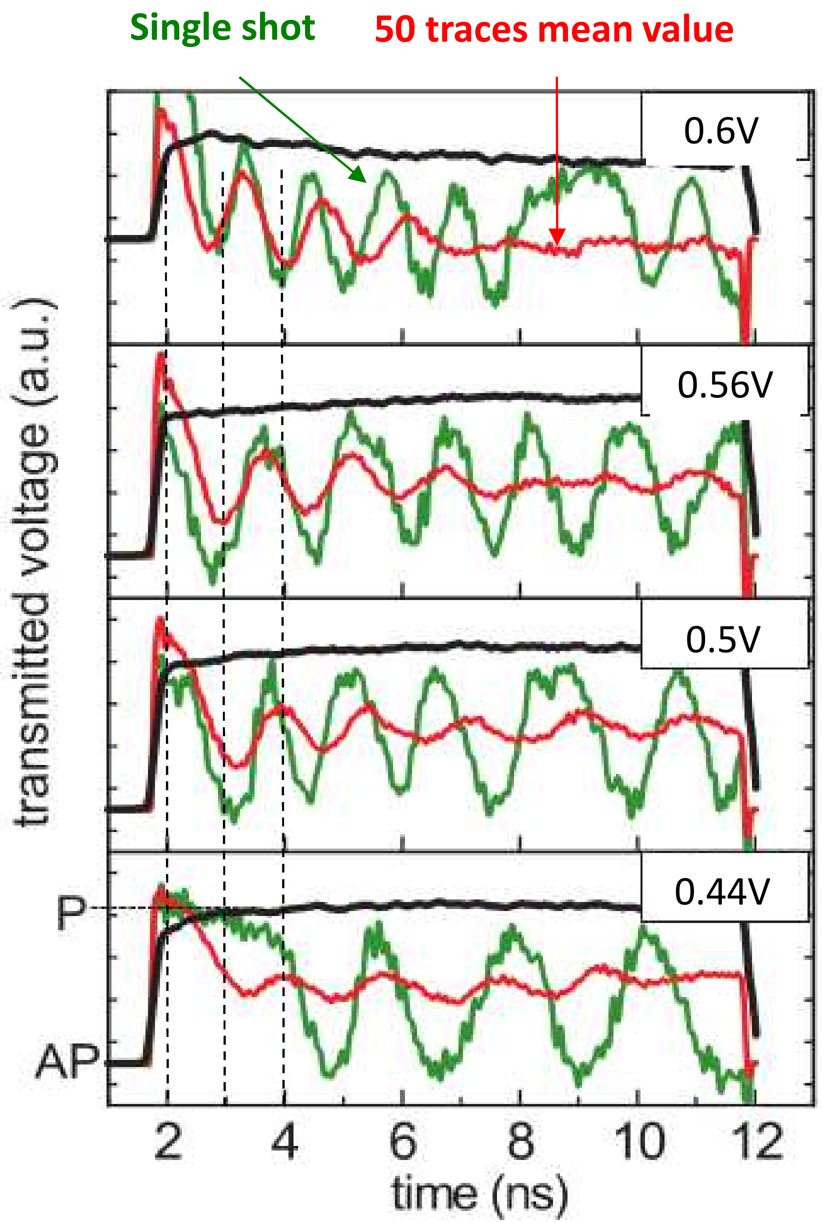




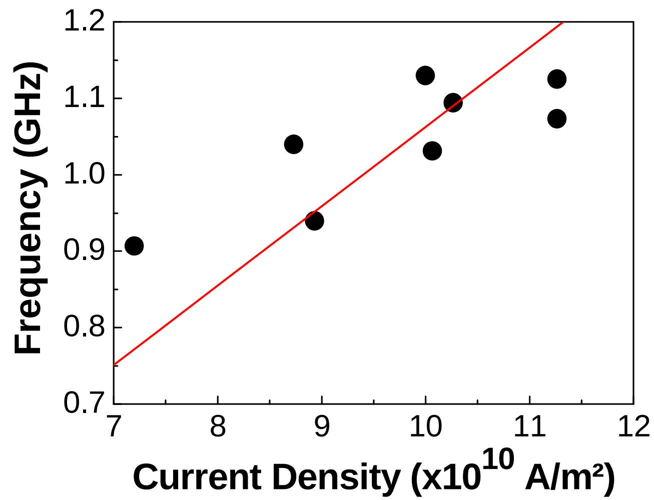


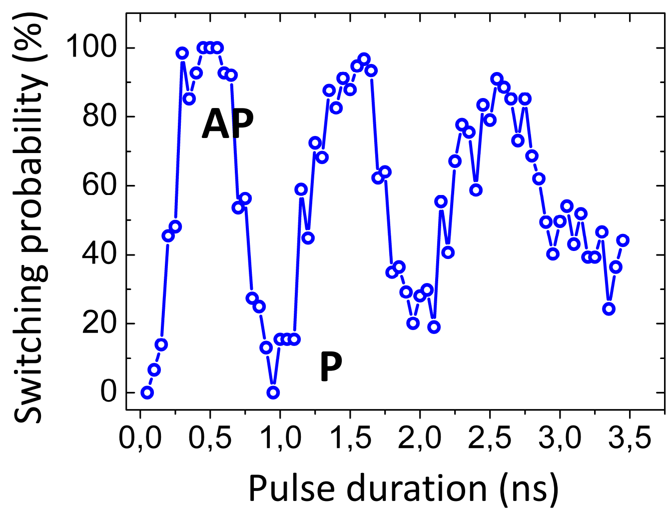
Real time measurements: T. Devolder (C2N)

A: Dynamics dominated by the STT contribution from perp polarizer (AR=2)



Cell size : 80nm x 160nm, 10ns pulses





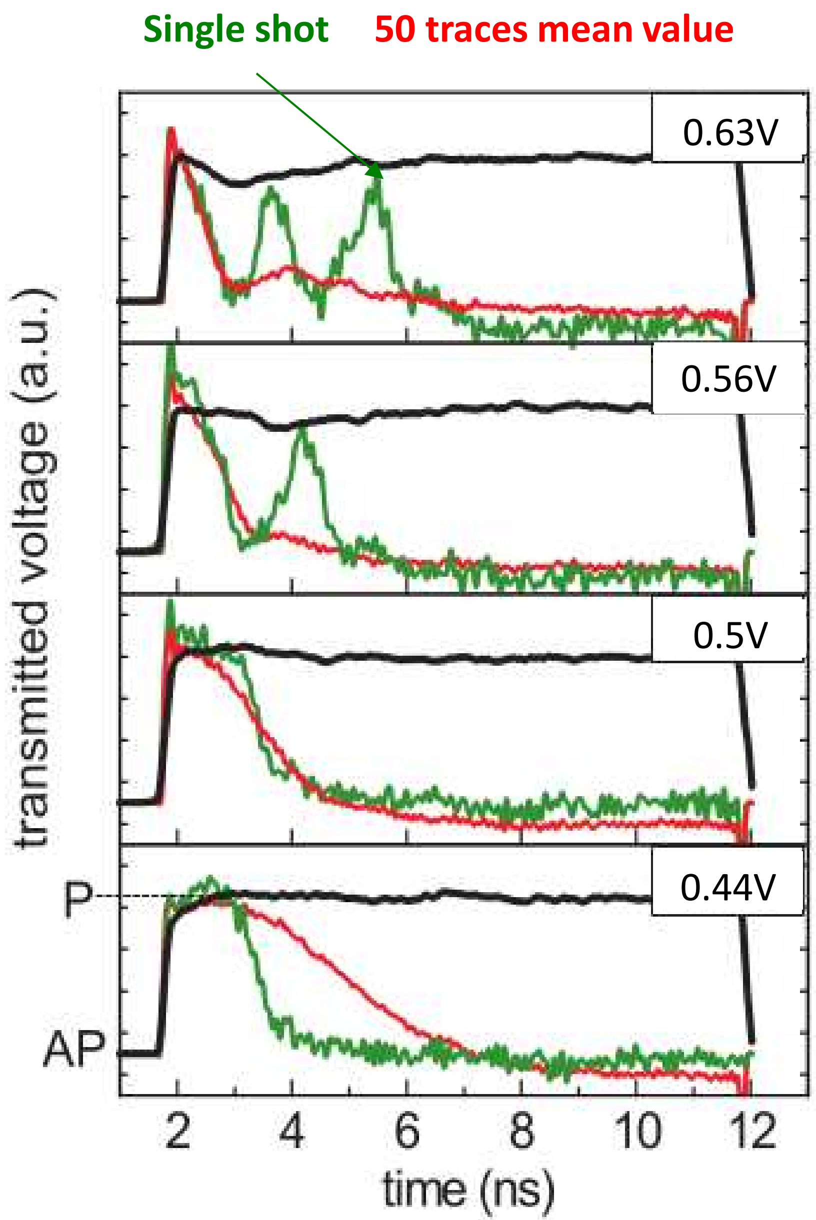
1. Precession frequency depends linearly on the current density

$$f \approx \frac{\gamma}{2\pi}\left[\frac{\hbar}{2e}\frac{g(\eta)}{M_s t}\right]\frac{J}{\alpha}$$

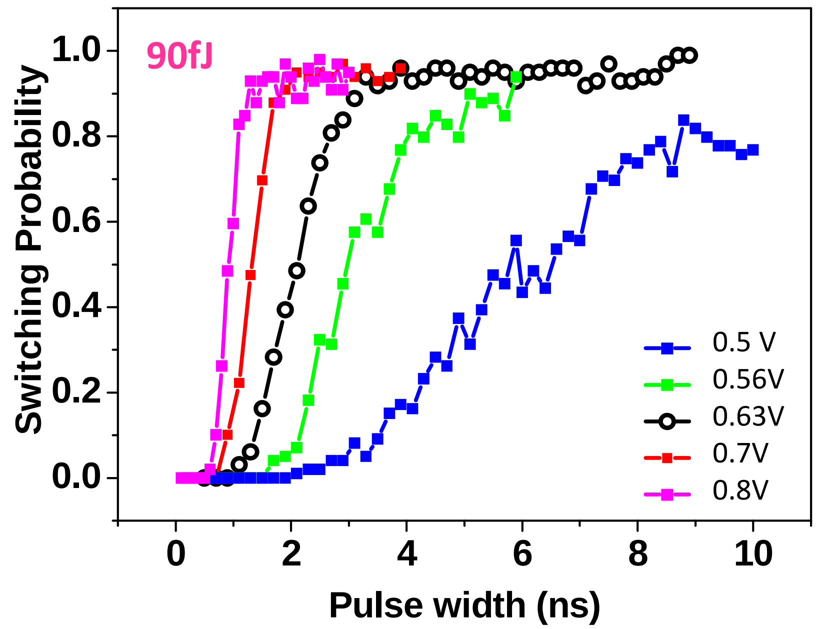
2. Dephasing of precessional motion in less than 10ns

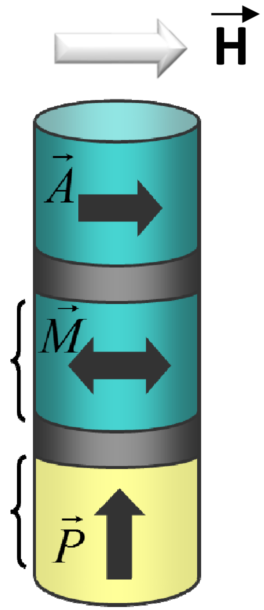
*Lacoste et al, PRB **89** (2014) 064408*
*Lacoste et al, PRB **90** (2014) 224404*
Lacoste et al, IMW 2016

B: Dynamics dominated by STT contribution from in-plane analyzer (AR=5)



Cell size : 50nm x 250nm





Large aspect ratio allows for non-oscillatory, fast and direct overwrite switching.

Precession stops at stable state after half a precession period

Large cells due to high required aspect ratio: is there another way to obtain the desired bipolar switching dynamics?

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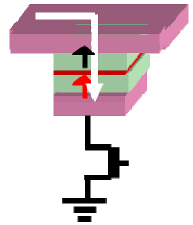

A.Timopheev et al, PRB 92, 104430 (2015)
A.Timopheev et al, Scientific Reports 6, 26877 (2016)

P-MTJ based on interfacial PMA (i-PMA)

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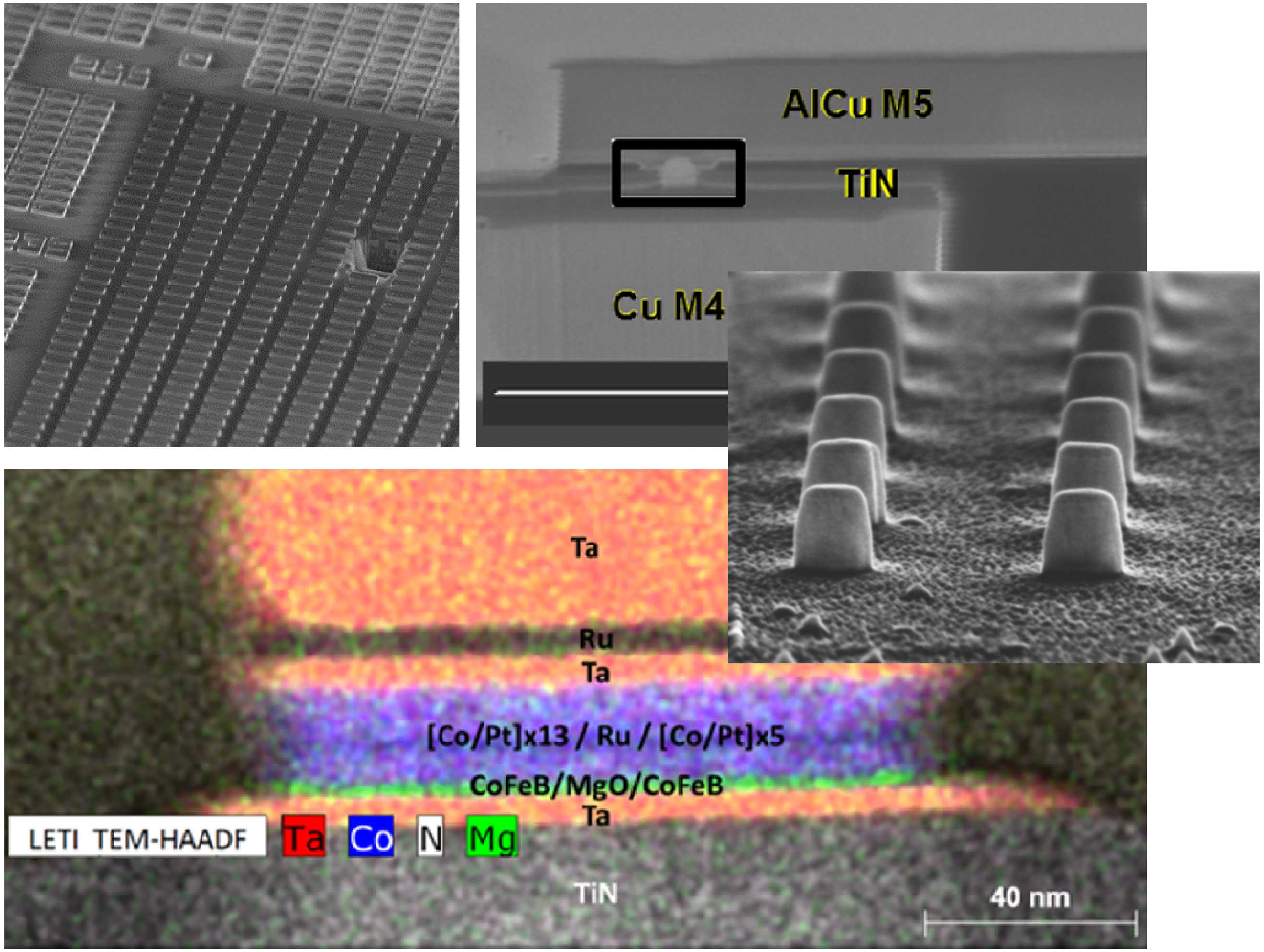
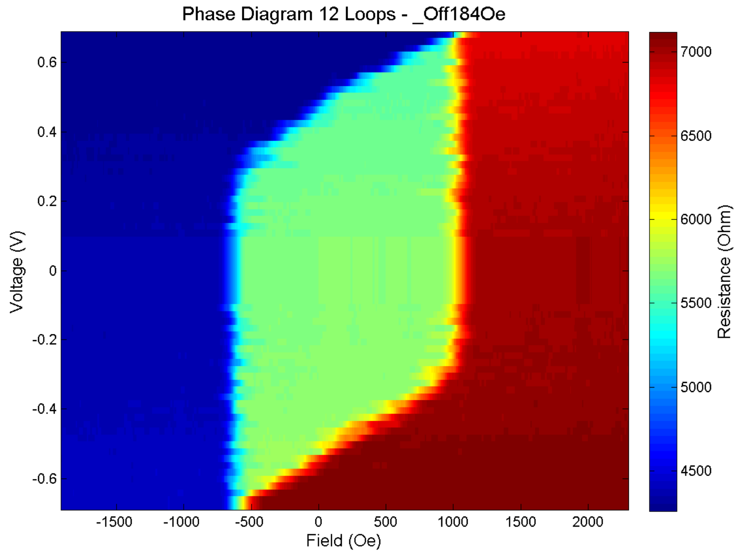
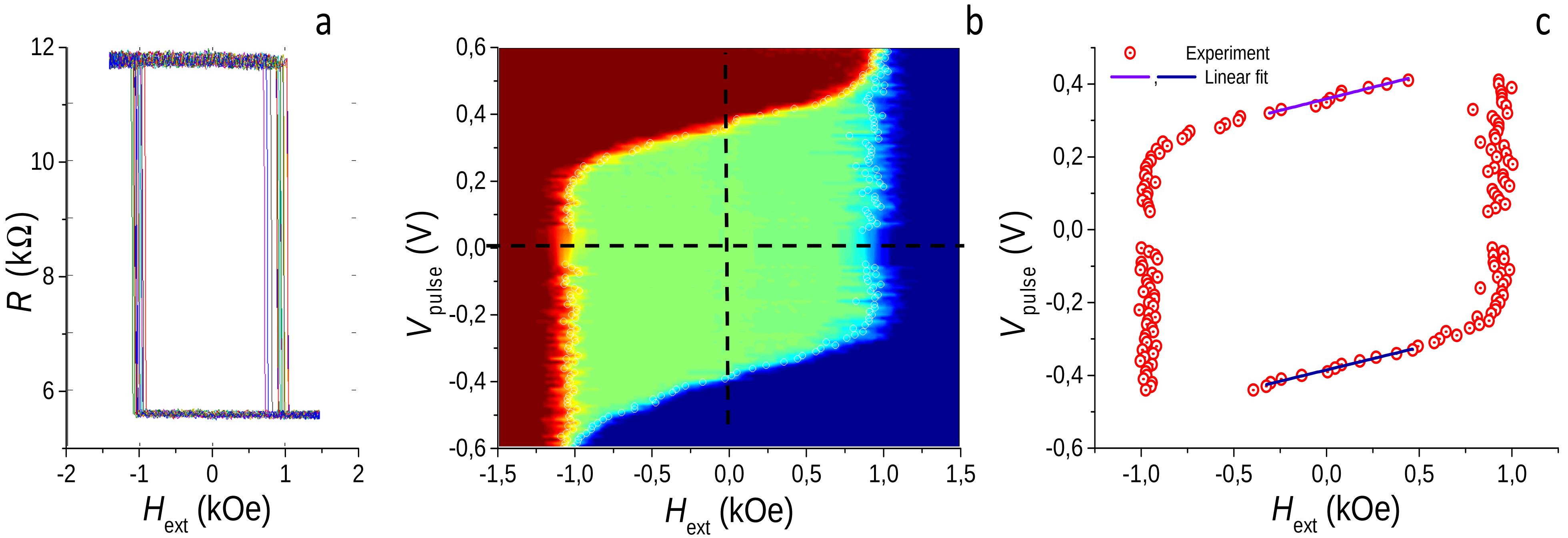




📖 *L. Tillie et al, Proceedings of IEDM (2016)*

Interfacial perpendicular anisotropy allows to obtain together good memory retention, high tunnel magnetoresistance for readout, low switching current during write

Perpendicular STT-RAM with 2nd order anisotropy



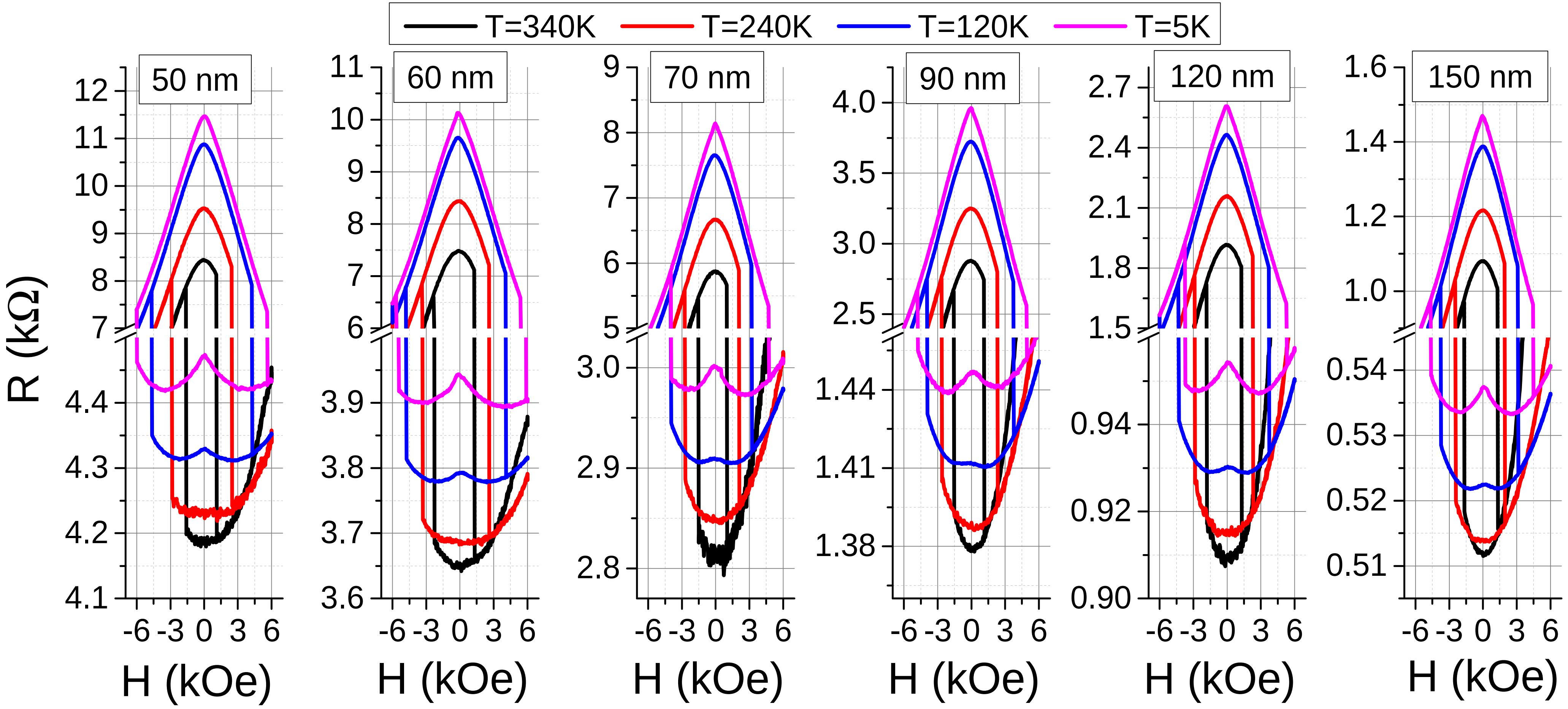
However, with easy-axis measurements only, uncertainty on the switching mechanism (nucleation/propagation or coherent rotation) and not much detailed information on the anisotropy itself

→ Better to use hard-axis measurements

A.Timopheev et al, PRB92, 104430 (2015).

A.Timopheev et al, Scientific Reports **6**, 26877 (2016)

Perpendicular STT-RAM with 2nd order anisotropy



hard-axis measurements

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Modelling hard axis R(H) curves by introducing a 2nd order anisotropy term $K_{2s}\cos^4\theta$ both in the free and reference layers

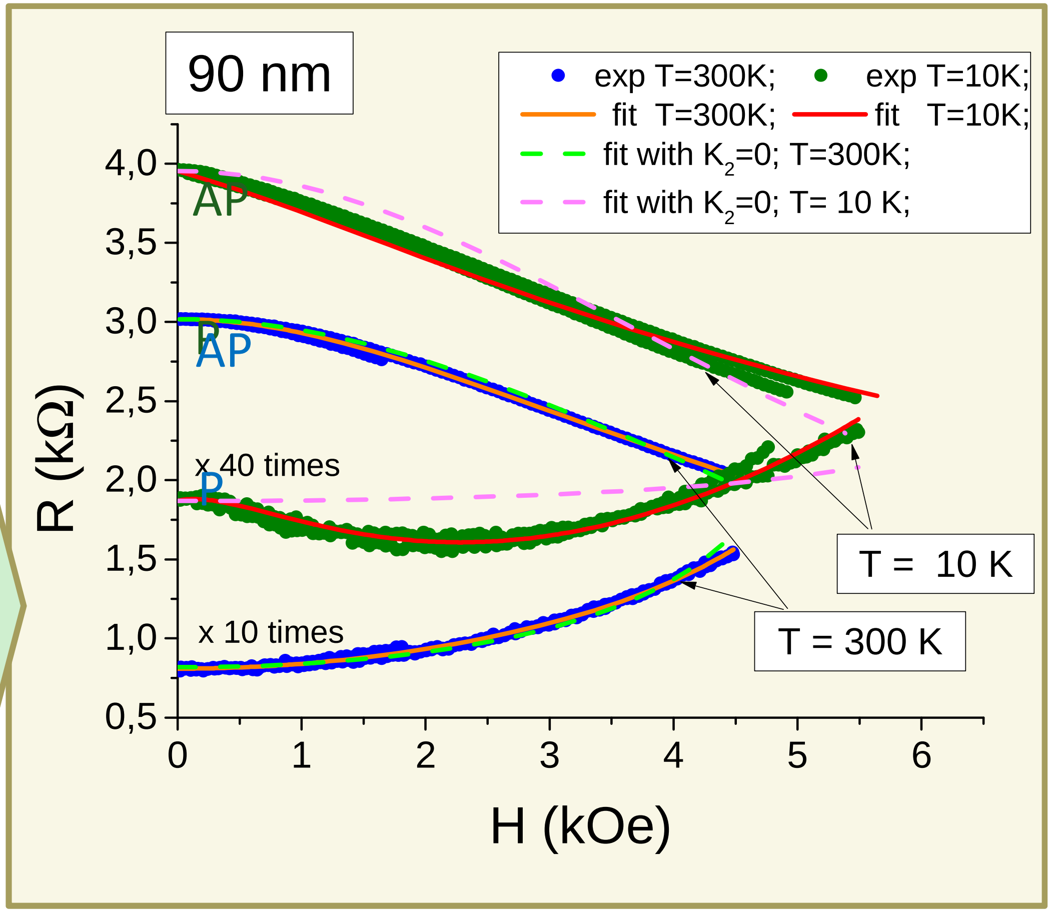
$$\frac{E_{tot}}{M_S} = -\frac{K_1}{M_S}\cos^2\theta - \frac{K_2}{M_S}\cos^4\theta - H\sin\theta.$$

T = 10K:

$\frac{K_{1F}}{M_S}$ =5184 Oe, $\frac{K_{2F}}{K_{1F}} = -0.2$; $\frac{K_{1R}}{M_S}$ =37285 Oe, $\frac{K_{2R}}{K_{1R}} = -0.514$

T = 300K:

$\frac{K_{1F}}{M_S}$ = 2815 Oe, $\frac{K_{2F}}{K_{1F}} = -0.104$; $\frac{K_{1R}}{M_S}$ =11084 Oe, $\frac{K_{2R}}{K_{1R}} = -0.265$



Use of 2nd order anisotropy in perpendicular STT-RAM

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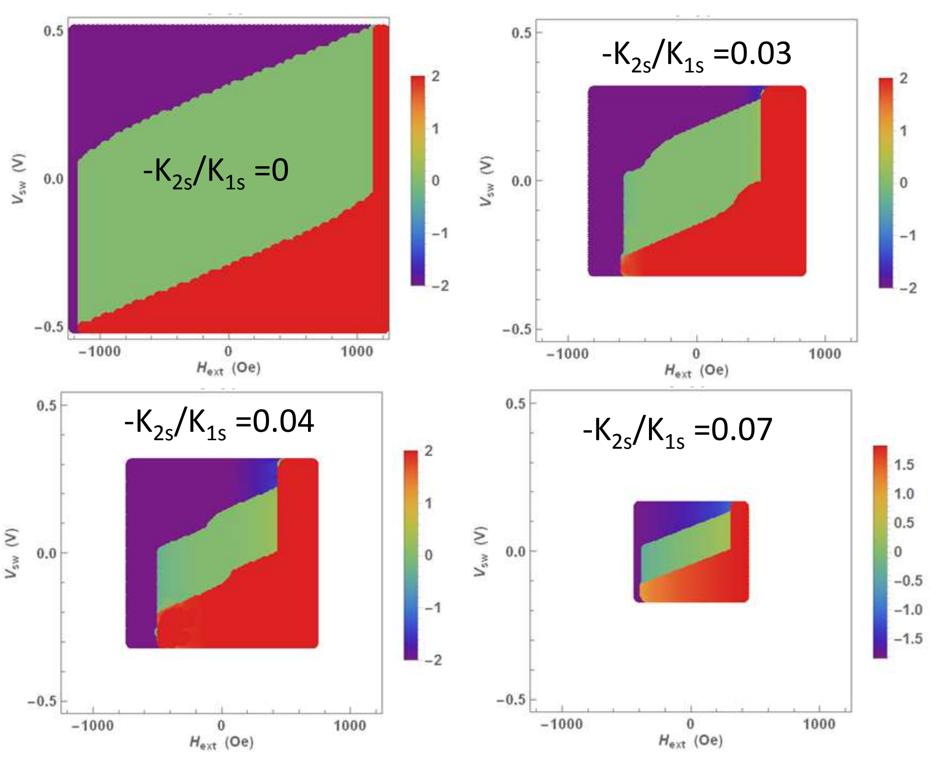
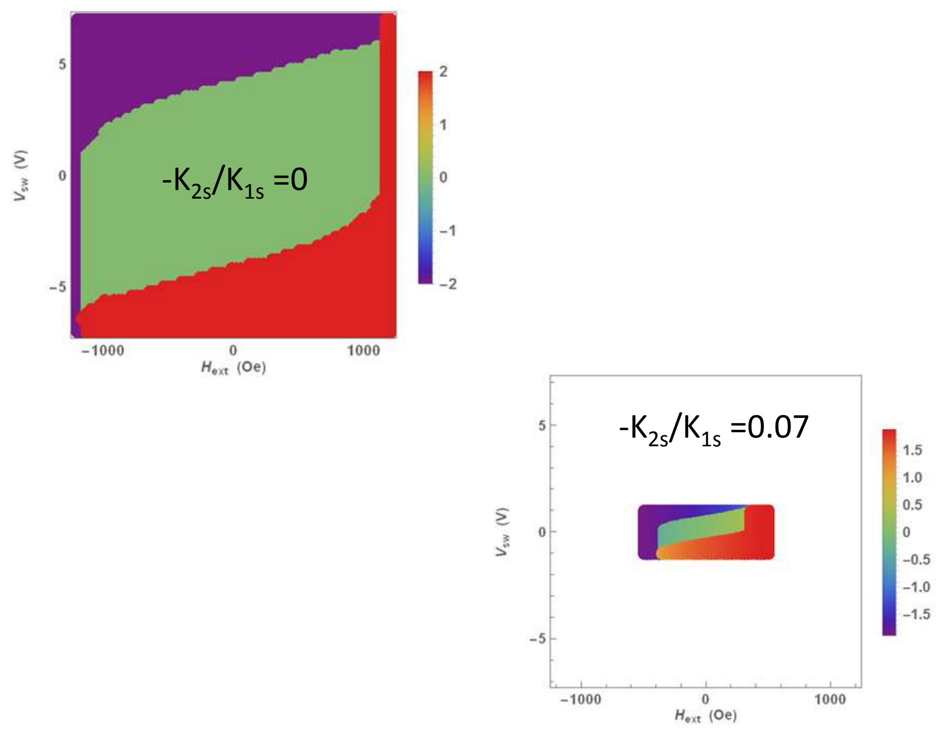
Write pulse duration = 50 ns



Write pulse duration = 1 ns



V_{sw} reduced ~ 4.8 times
H_{sw} reduced ~ 3.3 times

1.5 x in the Figure of merit I_{sw}/Δ

V_{sw} reduced ~ 8 times
H_{sw} reduced ~ 3.3 times

2.4 x in the Figure of merit I_{sw}/Δ

As K2/K1 increases, Δ ↘ but switching voltage decreases faster than retention →

Figure of merit I_{sw}/Δ ↗

Easy-cone regime provides initial angle which triggers magnetization reversal →

Fast switching

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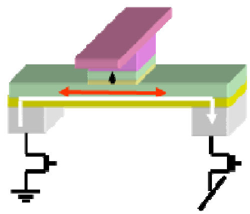
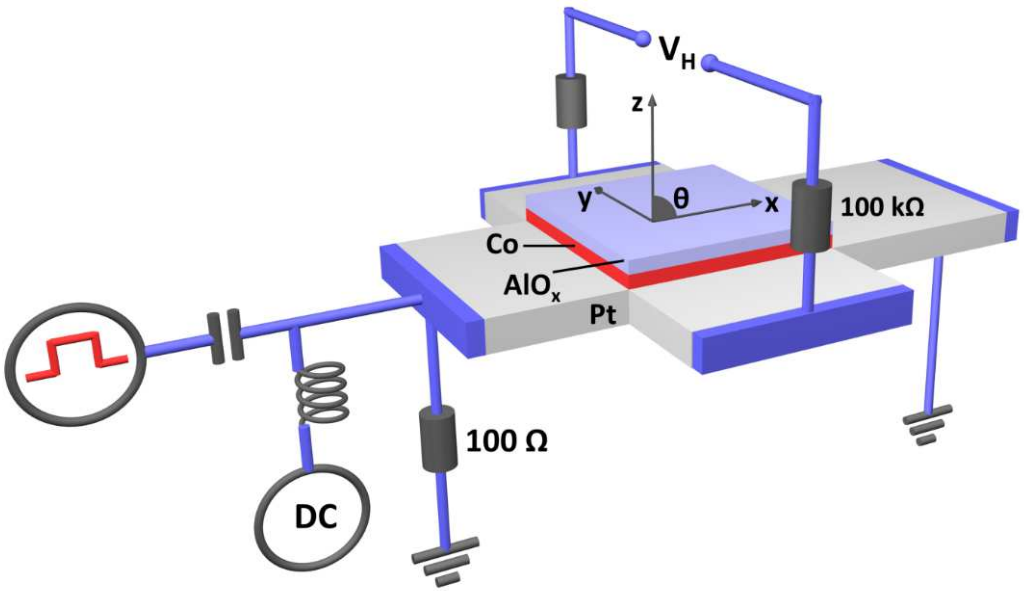
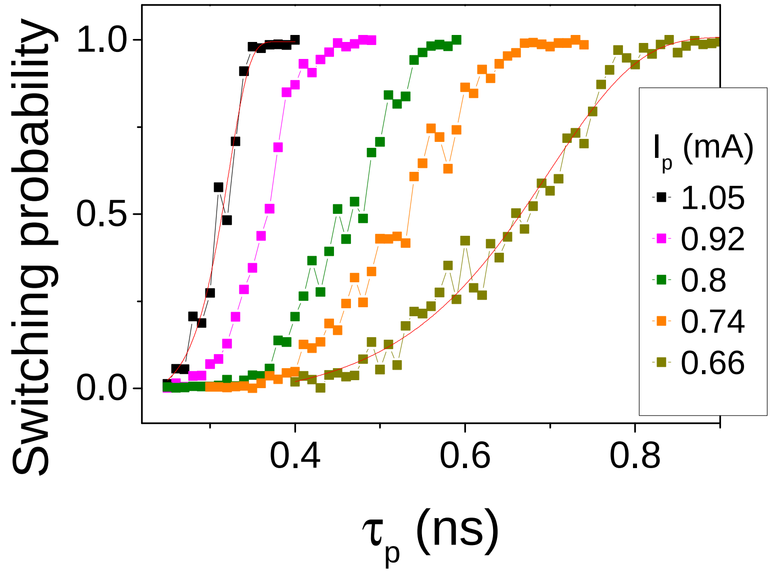


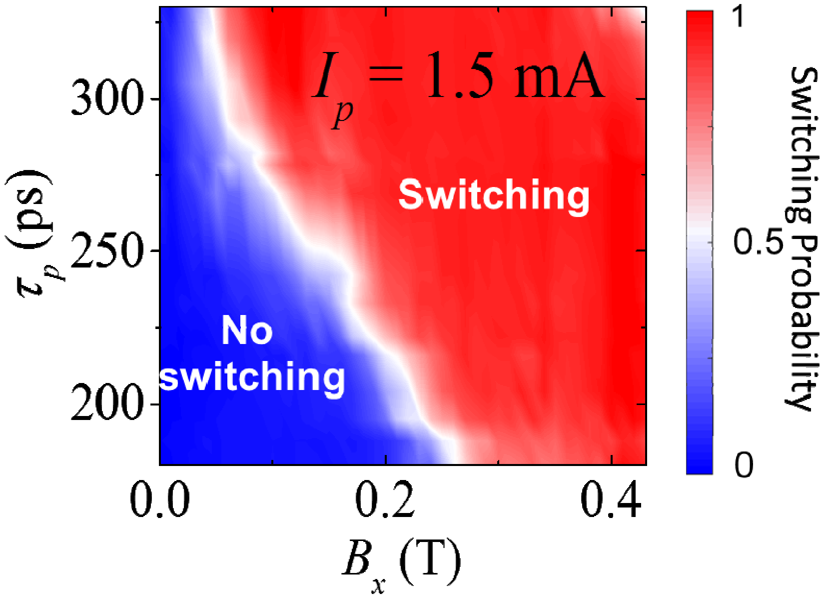
K. Garello et al., Appl. Phys. Lett., ***105****,212402 (2014)*

High speed SOT-MRAM





Switching for pulses down to 180 ps

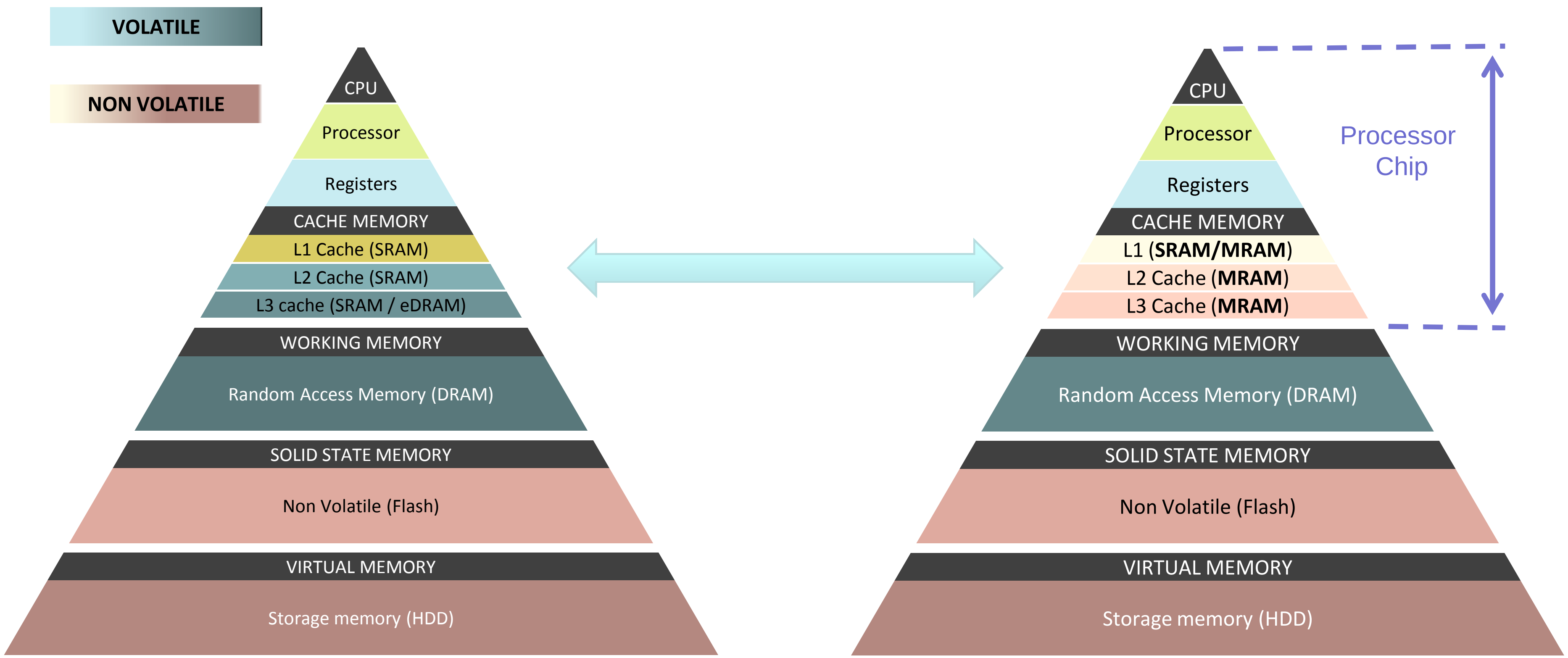


spintec SPOT ETH Zürich SINGULUS

Use of STT/SOT at the cache level

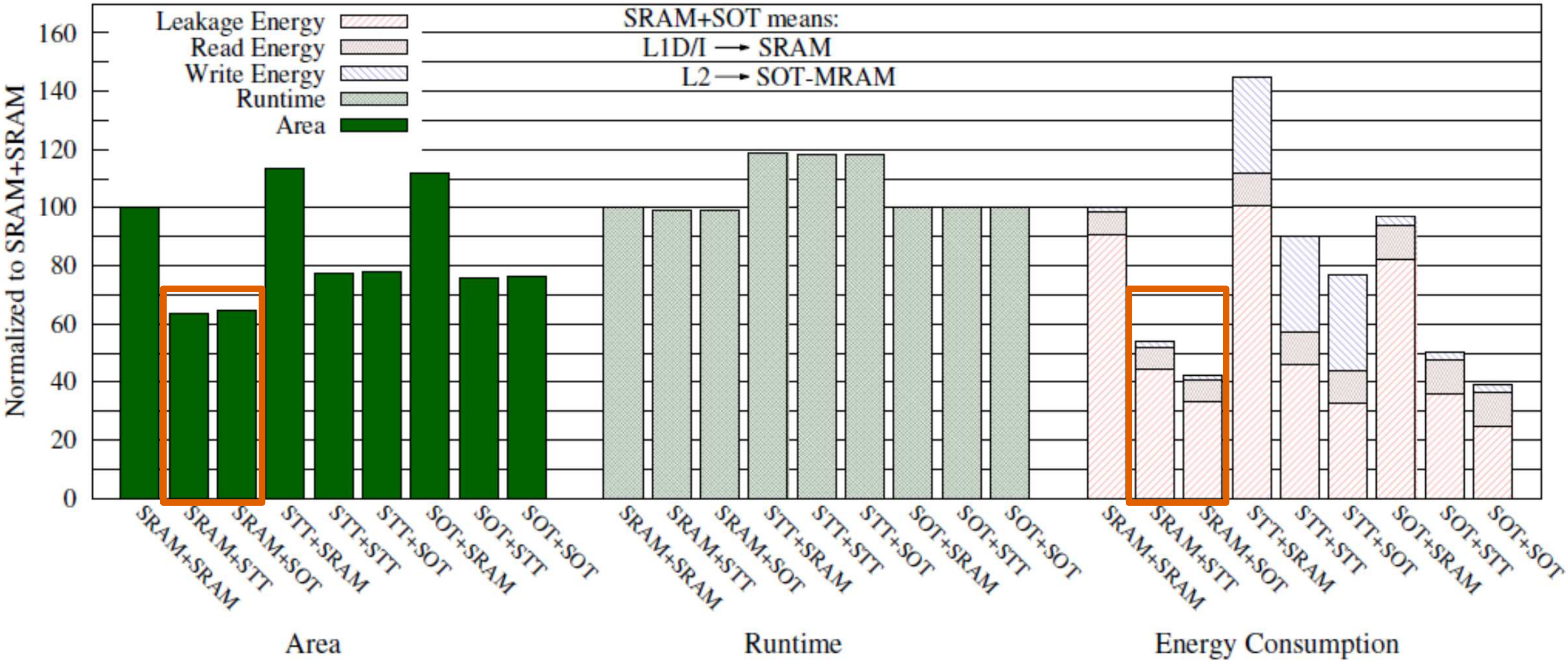
On-chip L1-L3 cache replacement with same overall architecture

→ *Single-core processor (3GHz) and pipeline based on Alpha 21 264 processor.*
→ *Cell-level information extracted using SPICE simulations*
→ *NVSimtool is explored to estimate the design data*
→ *Multiple applications run using GEM5 simulator*



F. Oboril et al., IEEE Trans. On Computer, **34,** 367 (2015)

Use of STT/SOT at the cache level



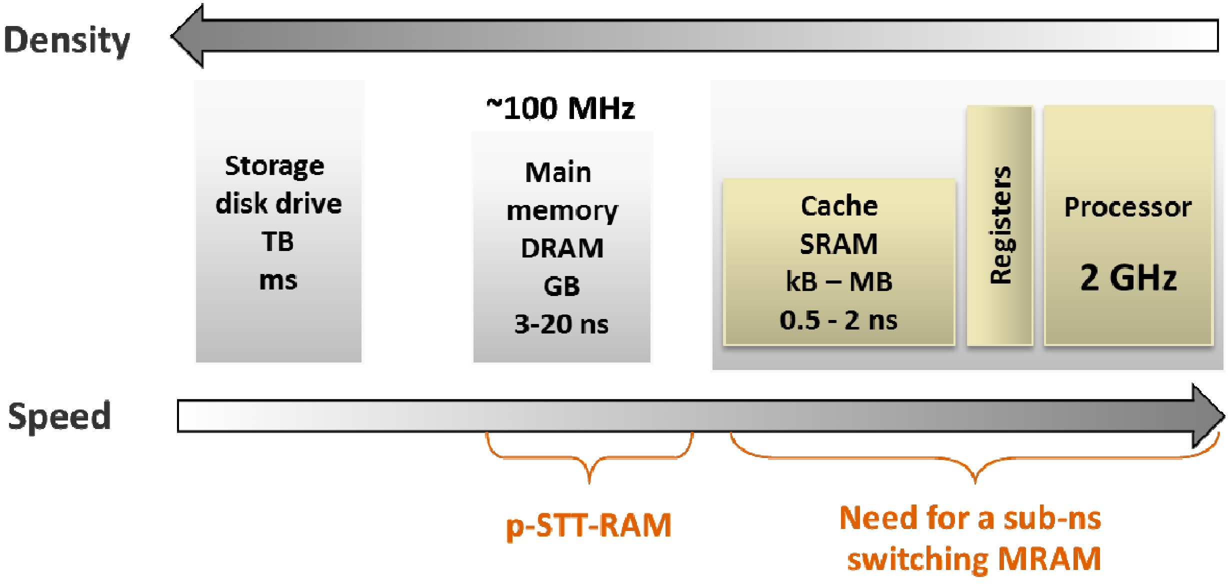
Best compromise SRAM L1 + SOT L2/L3 →

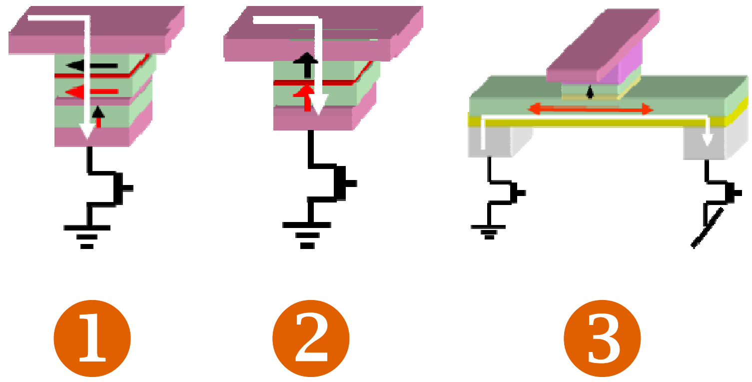
SPOT

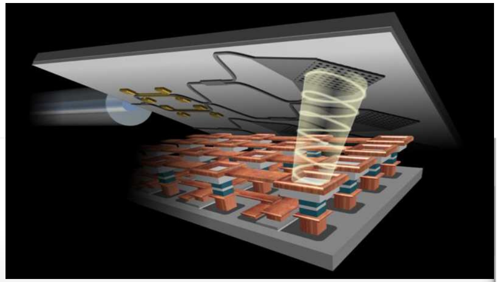
Energy consumption reduced by 60%
Area reduced by 30%
Performance similar to full-SRAM

F. Oboril et al., IEEE Trans. On Computers, **34,** 367 (2015)

Summary: *ultrafast MRAM concepts*







❶ **Low AR perpendicular polarizer – high speed 200ps, no direct overwrite**

final state depends on the initial state and the current pulse direction

For direct-overwrite:

cell aspect ratio AR > 5: fast direct overwrite (500ps, 90fJ) but LARGE cells

constant transverse field AR = 2, increased manufacturing complexity.

❷ "2nd order anisotropy" resulting from spatial fluctuations of 1st order anisotropy

can help increasing the switching speed and reduce stochasticity of the switching.

Remaining challenge: achieve large thermal stability factor together with “easy-cone” anisotropy.

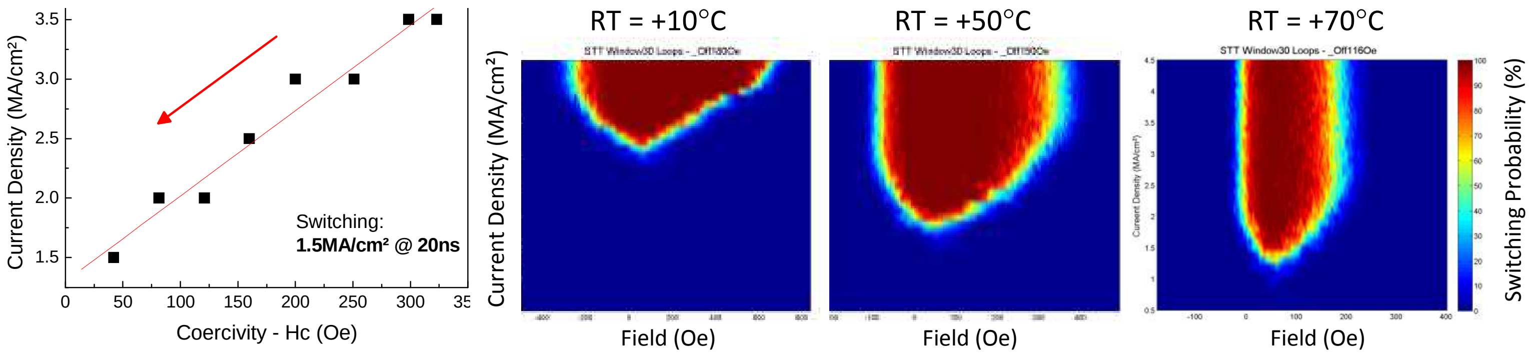
❸ Demonstration of functional non-volatile **three terminal SOT-MRAM single cell**

180ps write time demonstrated + **Switching deterministic**.

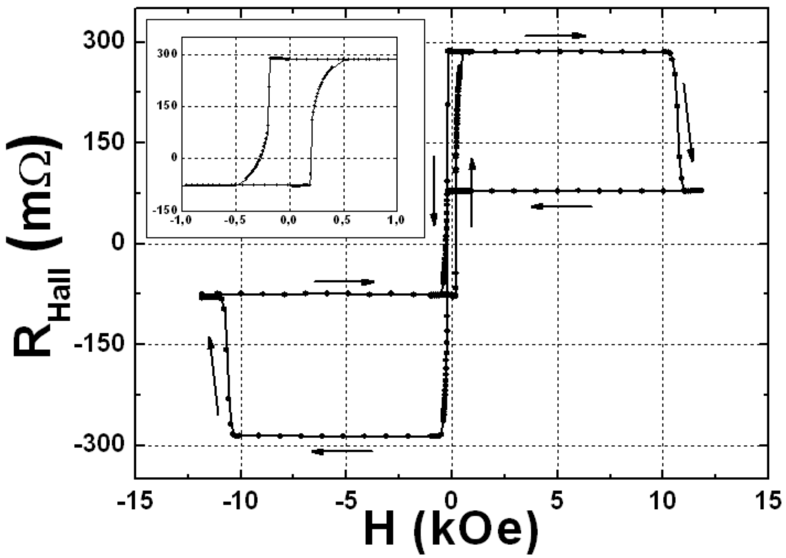
Remaining challenges: deterministic switching without external magnetic field / reduce writing current

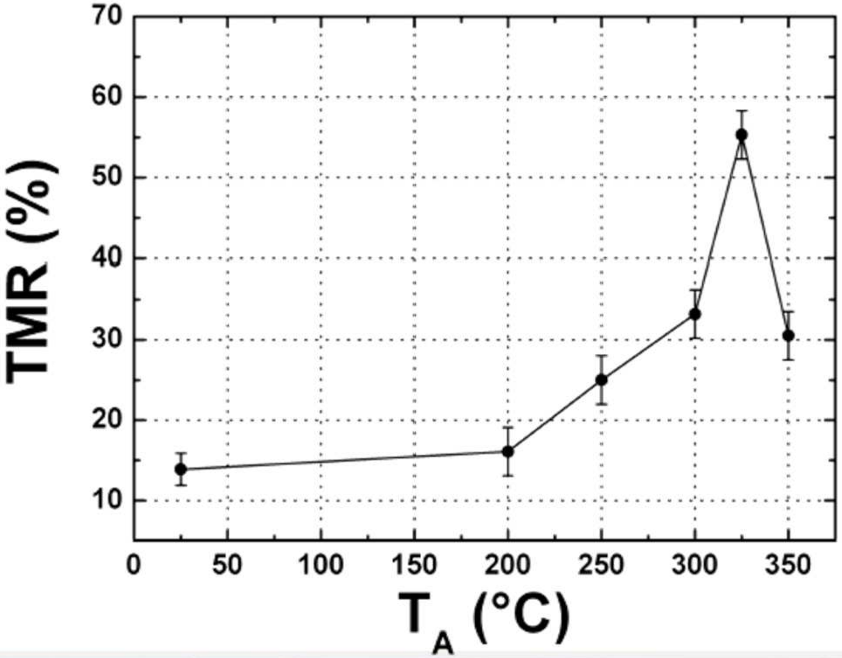
Electrical results – STT writing – influence of the heating

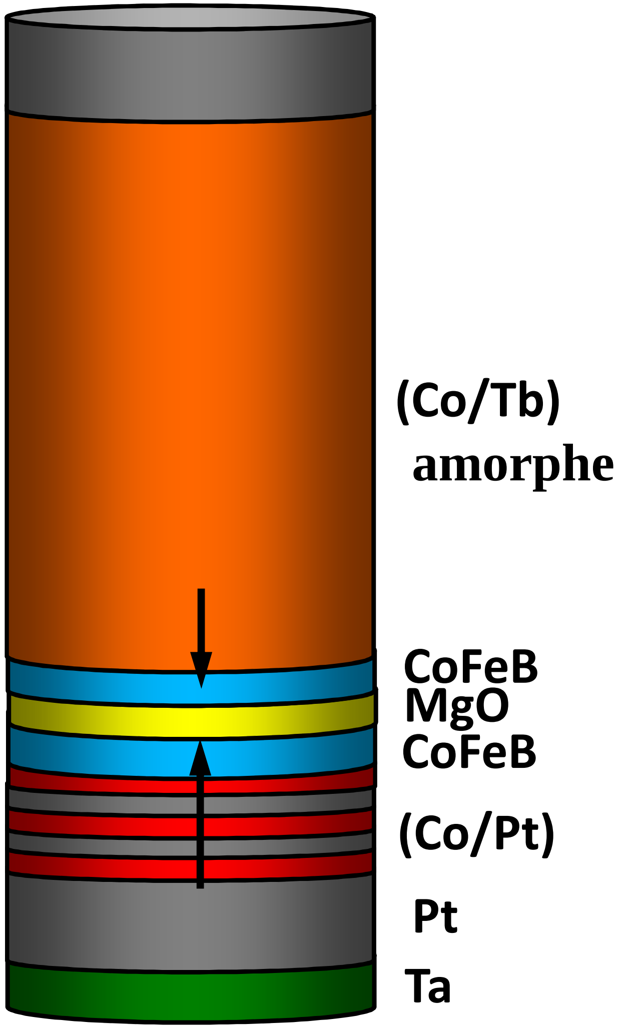
Thermal assistance also effective in perpendicular anisotropy from oxide interface



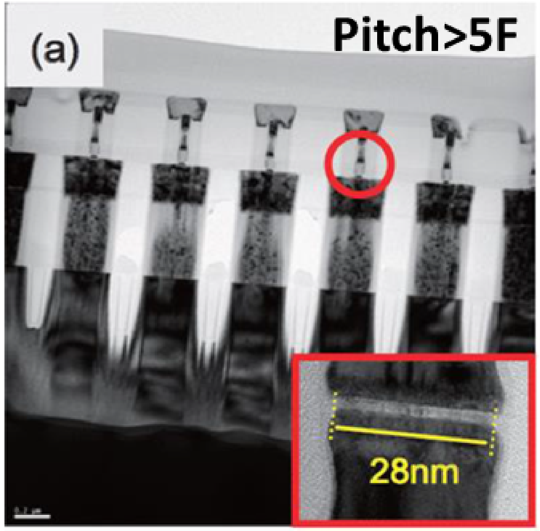
This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 713481.

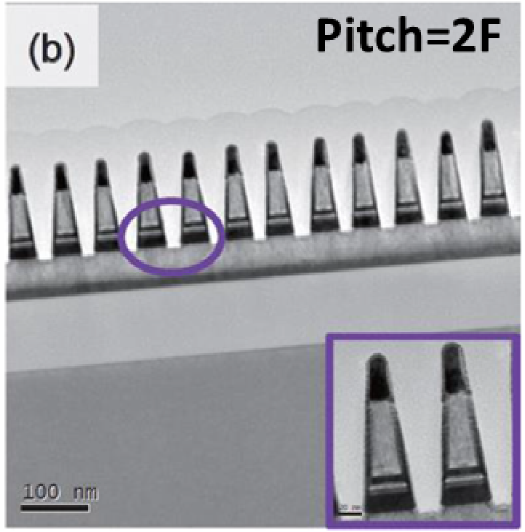

300
150
0
-150
-300
R_{Hall} (mΩ)
-15
-10
-5
0
5
10
15
H (kOe)


70
60
50
40
30
20
10
TMR (%)
0
50
100
150
200
250
300
350
T_A (°C)


(Co/Tb)
amorphe
CoFeB
MgO
CoFeB
(Co/Pt)
Pt
Ta

Nanopatterning of MTJ stacks **at very narrow pitch** using IBE



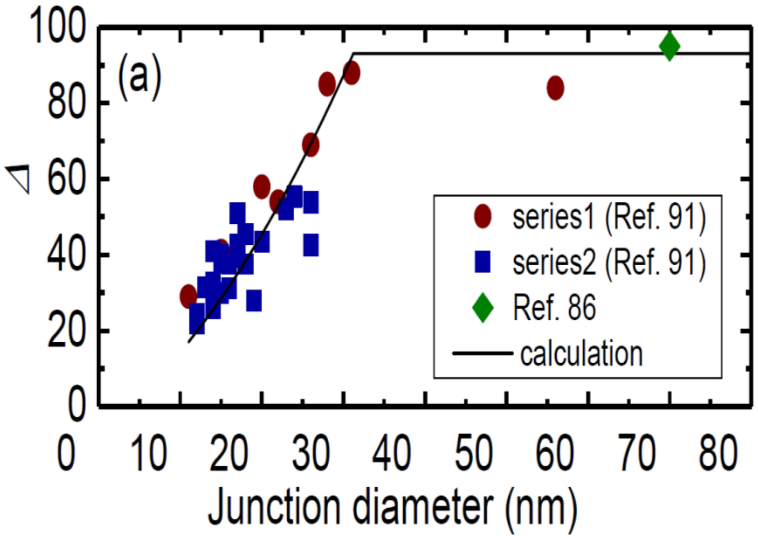


Well patterned

Shorts due to redeposition on sidewalls

Y. Kim et al, VLSI Symposium, pp. 210-211 (2011)
*V. Ip et al, IEEE Trans. Mag. **53,** 2400104 (2017)*

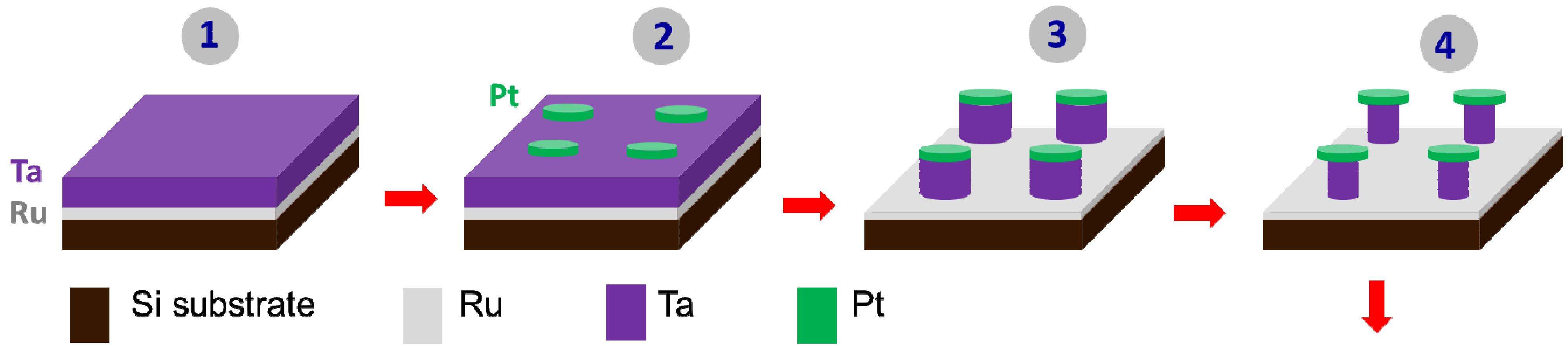
Large decrease in thermal stability factor at sub-20 nm



Insufficient memory retention

*L. Thomas et al, JAP **115**, 172615 (2014)*
*H. Sato et al, JJAP **56**, 0802A6 (2017)*

Fabrication of conducting non-magnetic posts by RIE

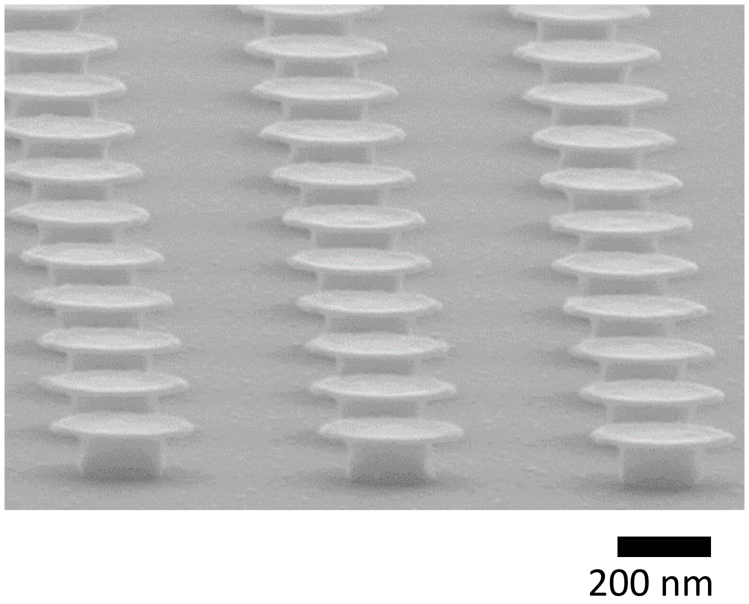


1. Deposition of Ru/Ta film on Si by sputtering

2. Definition of etching mask by e-beam lithography and lift-off process

3. Definition of Ta posts by anisotropic RIE

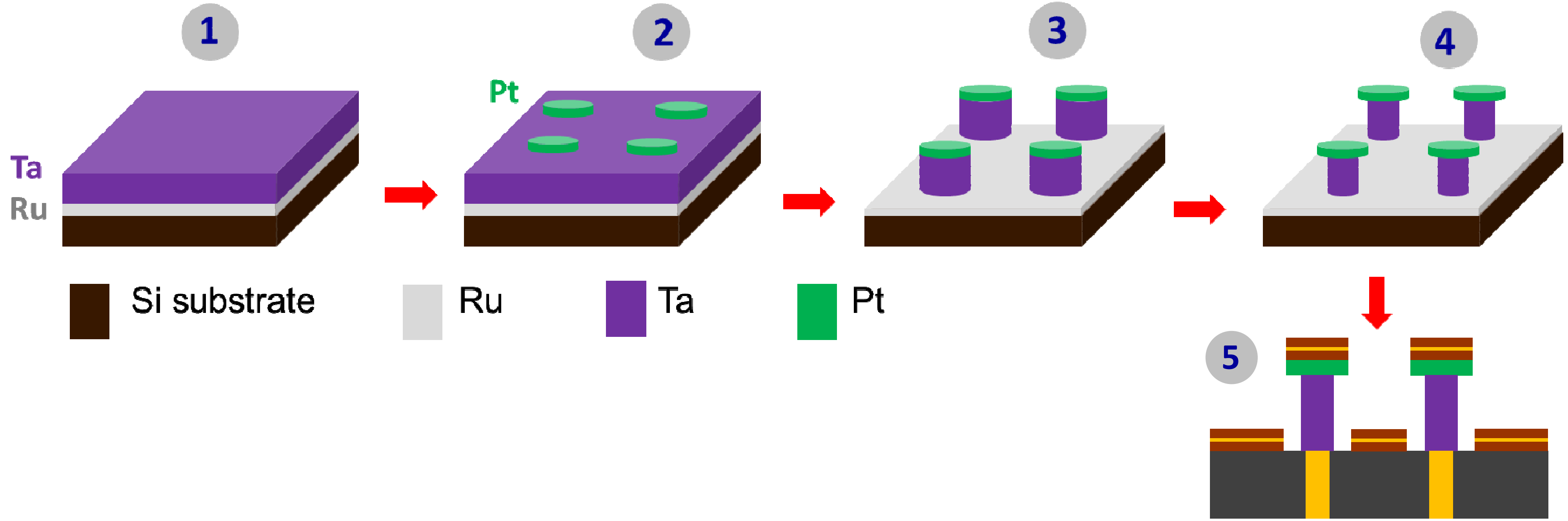
4. Definition of undercut of Ta posts by isotropic RIE

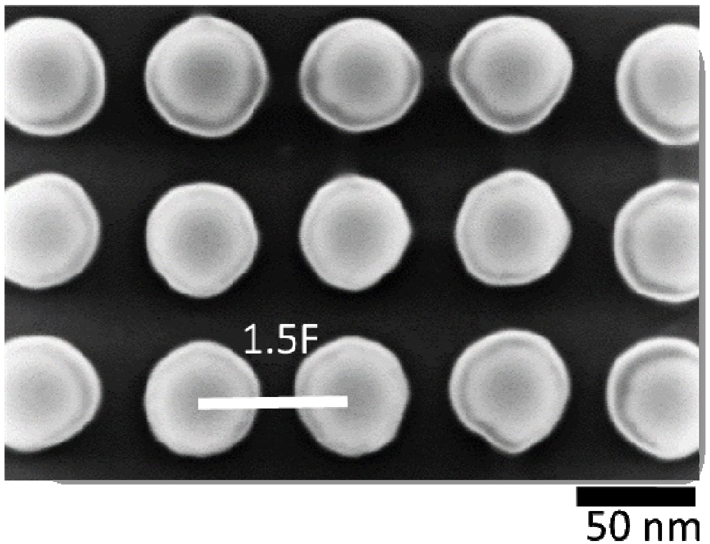


SEM image of Ta/Pt posts after RIE

The whole technological work was performed in our upstream research clean room facility (PTA) in Grenoble

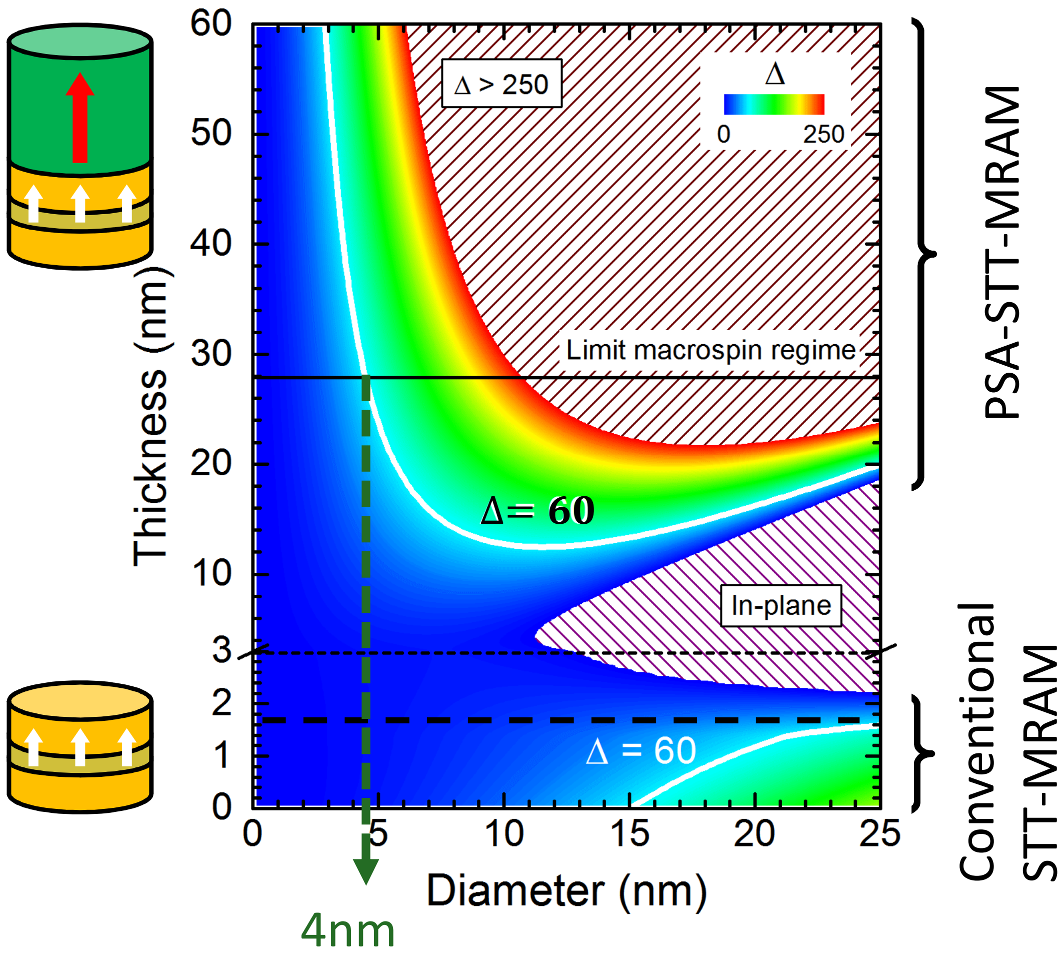
Fabrication of dense MTJ arrays (pitch down to 1.5F)





- ✓ This approach allows to fabricate extremely dense arrays of MTJs (1.5F pitch)
- ✓ Better use for fabrication of MTJs at dense pitch since less materials deposited on substrate
- ✓ Such dense arrays of MTJs have not been demonstrated so far with IBE approach (shadowing problem during etching)

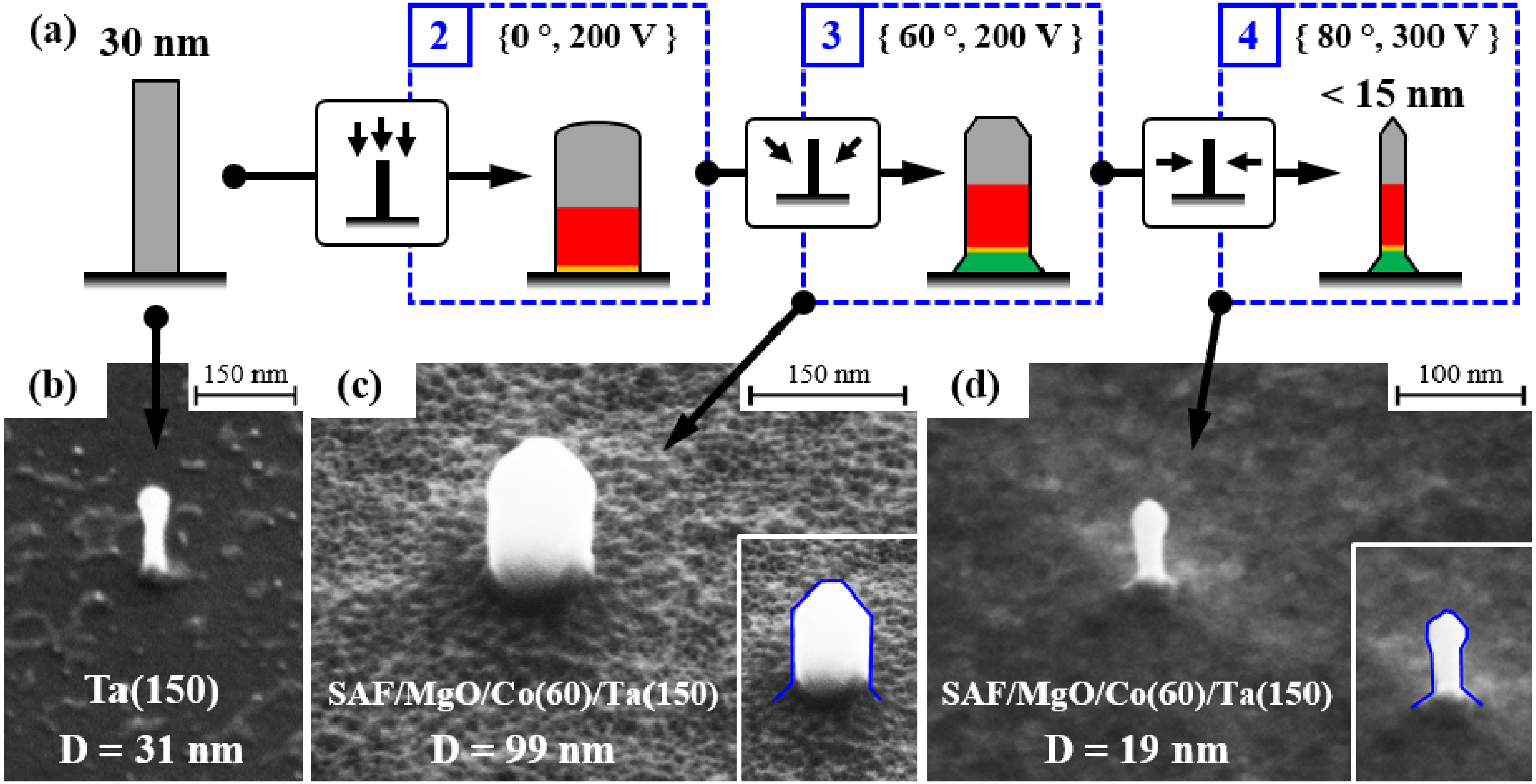
Thermal stability factor Δ vs. thickness and diameter



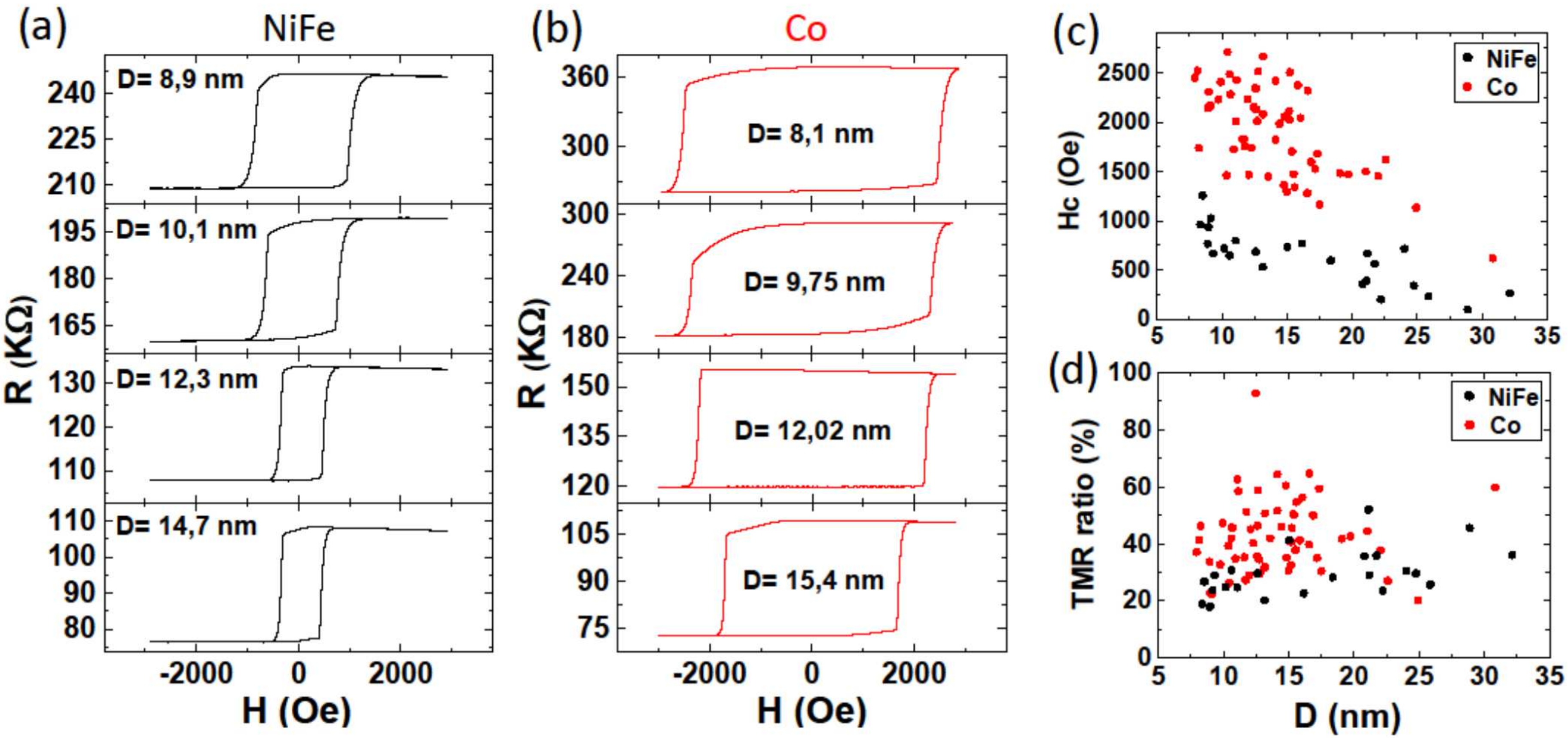
- ✓ Tunable thermal stability factor
- ✓ More robust source of anisotropy (bulk anisotropy)
- ✓ Weaker thermal variation of TMR and anisotropy thanks to much thicker storage layer.
- ✓ Use of lower damping materials possible and reduced spin-pumping effect.
- ✓ Extreme scalability (Δ>60 down to 4nm diameter)
- ✓ More challenging for nanoprocessing

N.Perrissin et al, Nanoscale 2018

PSA-STT-MRAM fabrication : *Etching & Trimming by IBE*

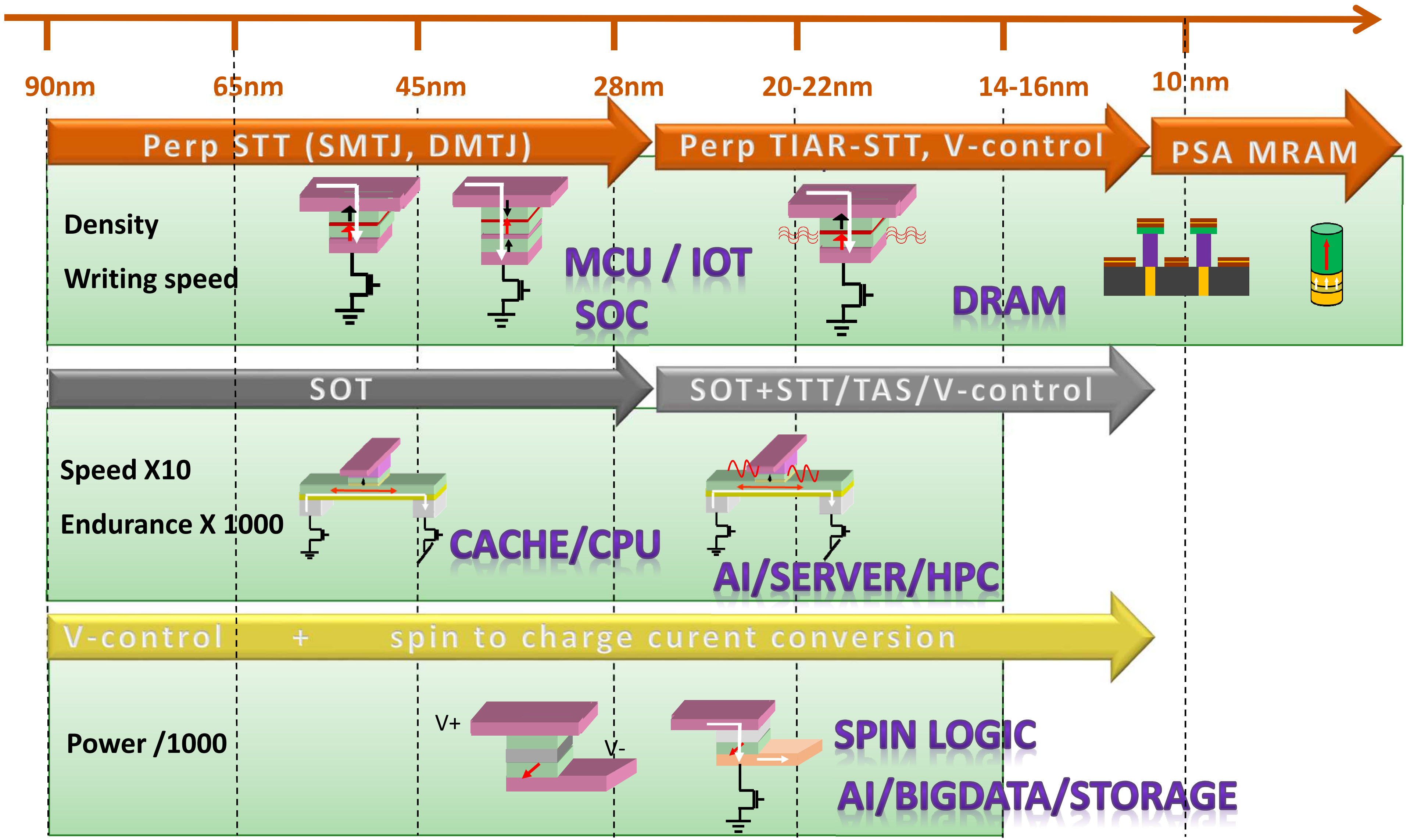


PSA-STT-MRAM : *electrical characterization R(H)*



Stack : SyAF/MgO/FeCoB 1.4nm/Ta0.2nm/(NiFe or Co – 60nm thick)

Spintronic – Application roadmap



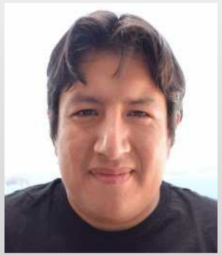
Thanks to

Simulation & theory

STT All optical PSA-MRAM DMTJ neurom



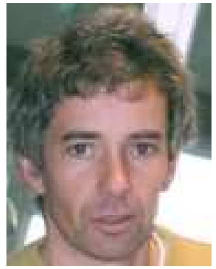



patterning

MSS

TEM



Materials


Nanofabrication




Test

Thank you for your attention !

www.spintec.fr

email: lucian.prejbeanu@cea.fr