SPICE Workshop
Antiferromagnetic Spintronics: from topology to **neuromorphic computing**
Schloß Waldthausen, Mainz, Germany
October 7th - 10th 2019

- Tutorial -

Neuromorphic Computing with Spintronics

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[Special thanks]
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Outline

0. Preface
1. General introduction to neuromorphic computing
2. Status and prospect of spintronics
3. Recent example: probabilistic computing using stochastic magnetic tunnel junction
4. Conclusion

Definition of terms

- **Neuromorphic computing**
  - [Narrow sense]
    Computing using analog circuits that mimic dynamics of nervous system
    Proc. IEEE, 78, 1629 (1990)
  - [Broad sense]
    Computing inspired by neuro-biological architecture ← **Today's definition**
- **Brain-inspired computing**
  - *Computing inspired by brain (no strict definition)*
- **Artificial intelligence**
  - [Narrow sense]
    Machines with software emulating mechanism of brain ← **Today's definition**
  - [Broad sense]
    Intelligent machines that work and react like humans

Motivation of neuromorphic computing

1. Engineering aspect

← **Today's standpoint**

- try to make computer efficient **like brain**
  (capable of executing complex tasks at low power level)

2. Brain-scientific aspect

- try to understand information processing **in brain**

3. Biomedical-engineering aspect

- try to communicate **with brain**
  (e.g., suppression of brain disorder)

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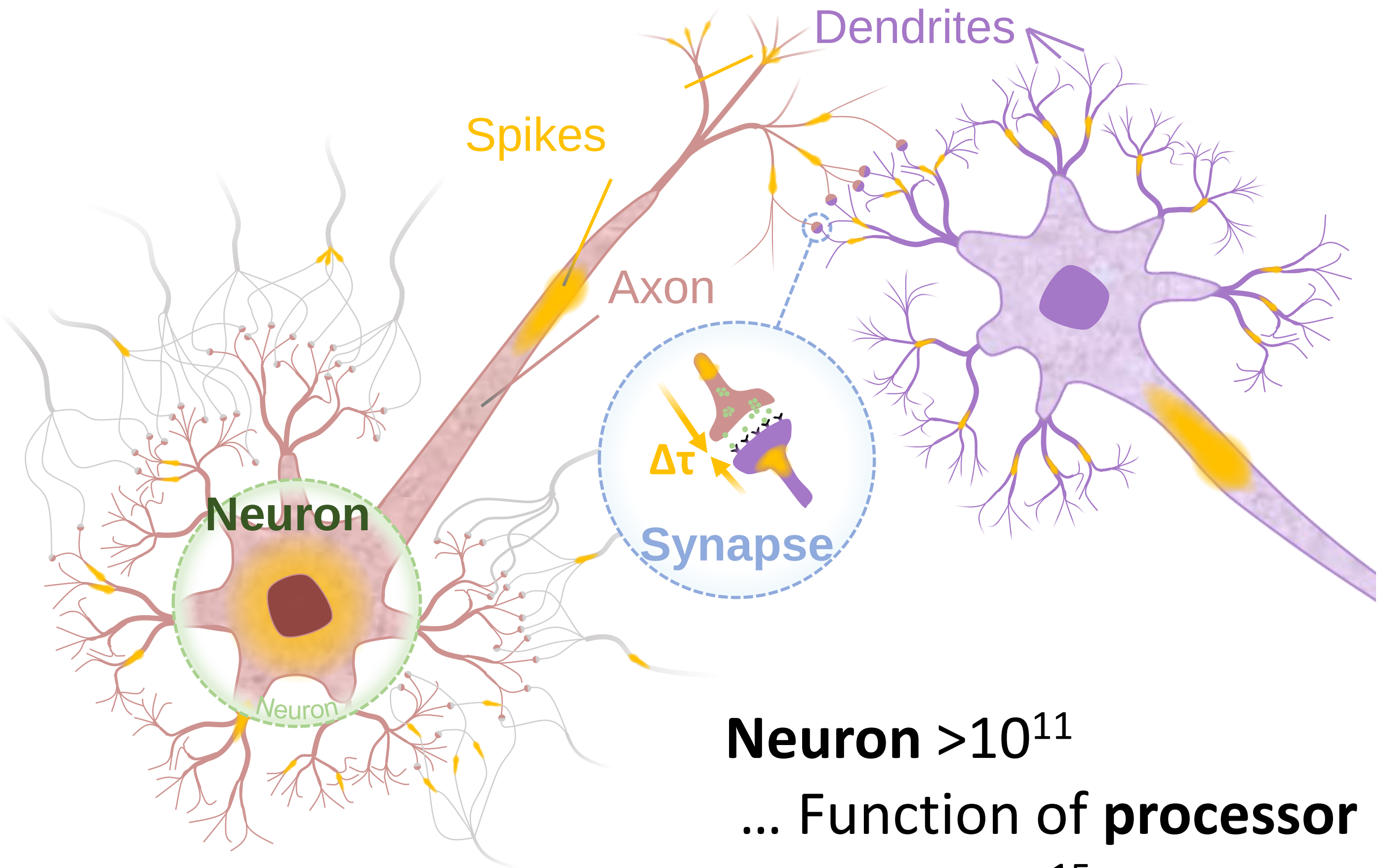
How different?

Classical computer	Brain
GHz	kHz
Digital	Analog
Rigid hierarchy	disorder
Clock driven Synchronous	Event driven Asynchronous
Sequential	Parallel
Logic/memory separation (von Neumann architecture)	In-memory computing
Minimum redundancy	Highly redundant (10^5 neurons die per day)
Good at well-defined problems, iterative tasks, …	**Good at ill-posed problems, cognitive tasks, …**

Fundamental units – neuron and synapse



Neuron $>10^{11}$

… Function of **processor**

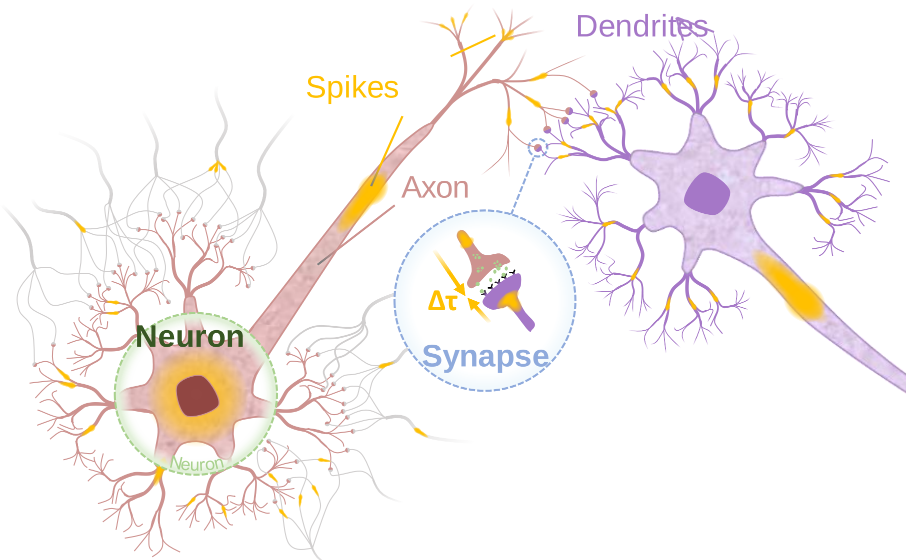
Synapse $>10^{15}$

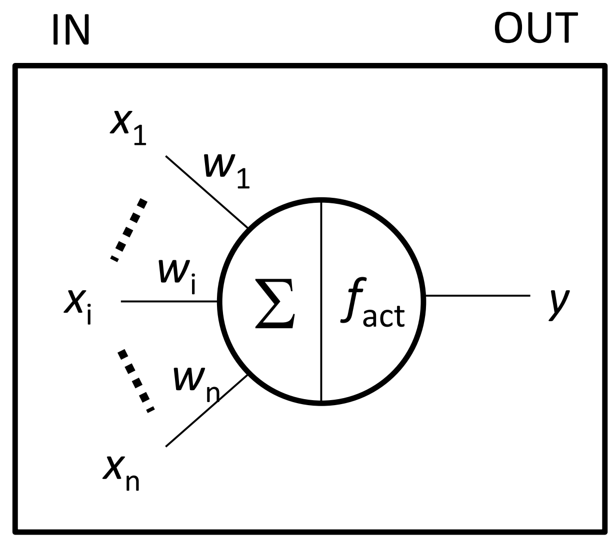
… Function of **memory**

➔ **Needs to reproduce by some means**

Fundamental units – neuron and synapse

Statically … Product-sum operation





$$y = f_{\mathrm{act}}\left(\sum_{i=1}^{n} x_i w_i\right)$$

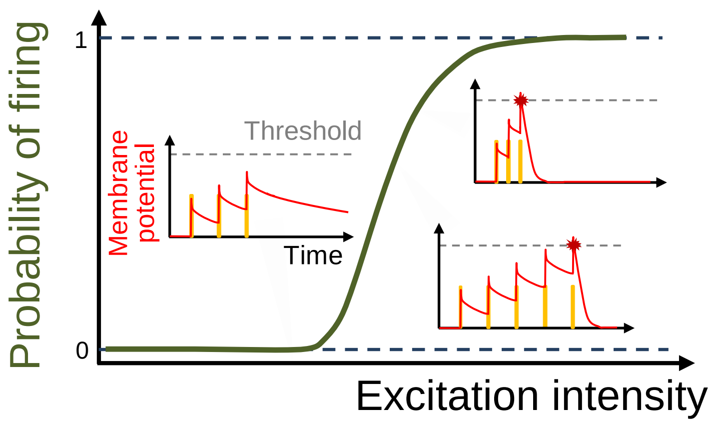
f_{act}: signum or sigmoidal function

Basis for Deep Neural Network (DNN), Convolutional Neural Network (CNN)

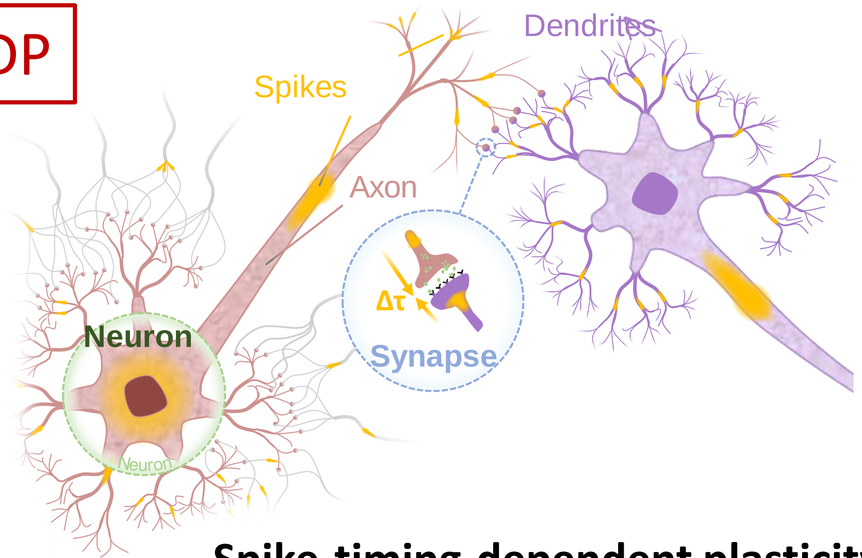
Fundamental units – neuron and synapse

Dynamically … LIF and STDP

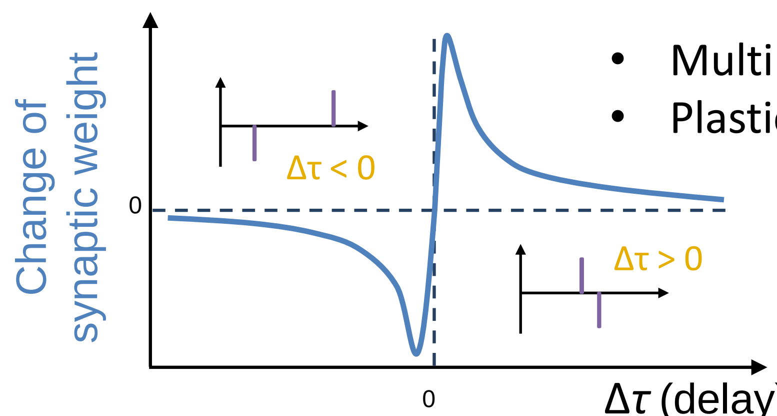
Leaky Integrate-and-Fire (LIF)



- Binary (Fire/Non-fire)
- Volatile (Leaky)



Spike-timing-dependent plasticity (STDP)



- Multilevel
- Plastic

Basis for Spiking Neural Network (SNN)

… event-driven asynchronous operation

Options for neuromorphic computing

<u>**Model**</u>

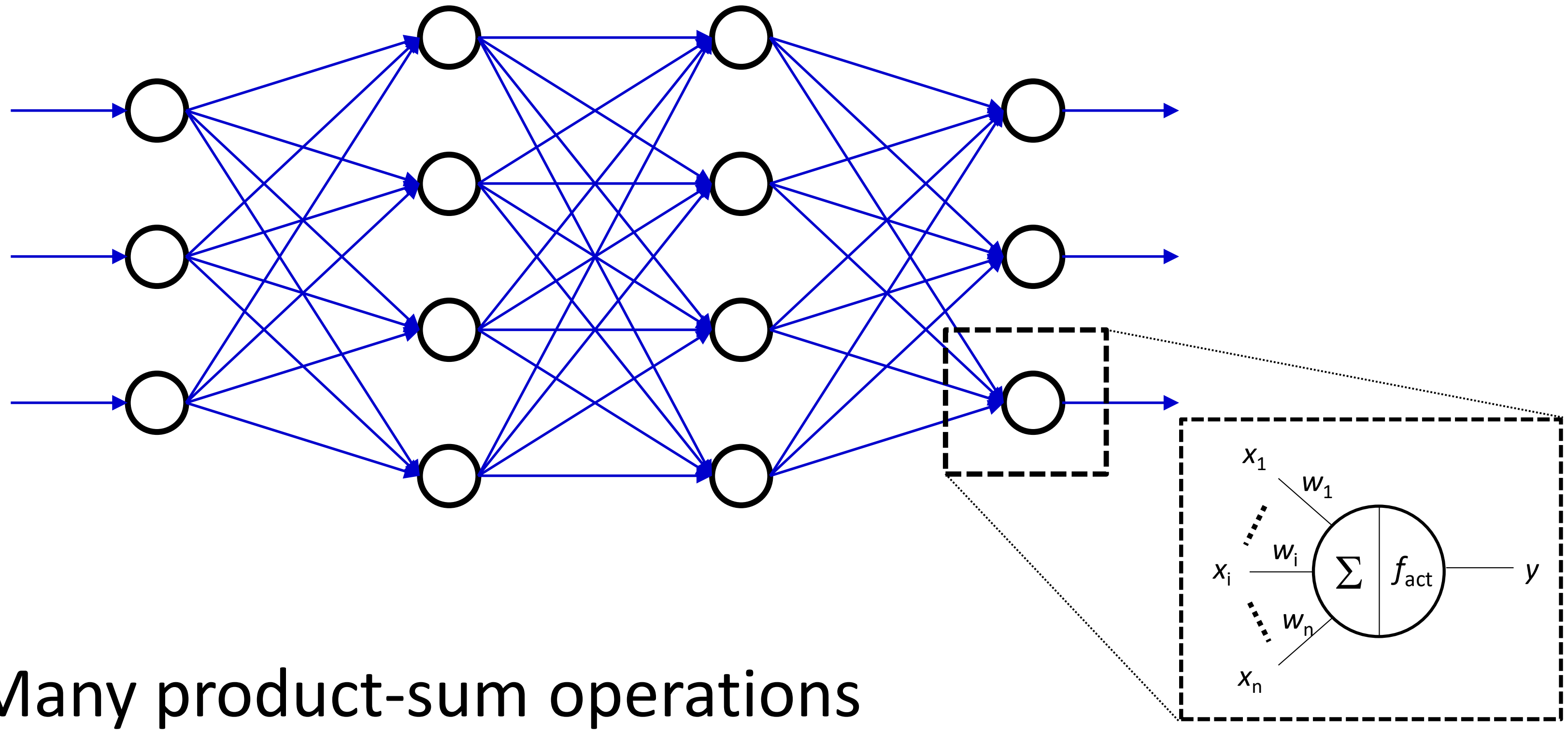
- Deep neural network
- Recurrent neural network
  - Reservoir computing
- Hopfield network
- Stochastic neural network (Boltzmann machine)
- Spiking neural network
- …

<u>**Hardware**</u>

- Conventional (von Neumann) computer
- CMOS-based sophisticated hardware
- CMOS + nonvolatile memory
- Synapse-like and/or neuron-like emerging devices
- …

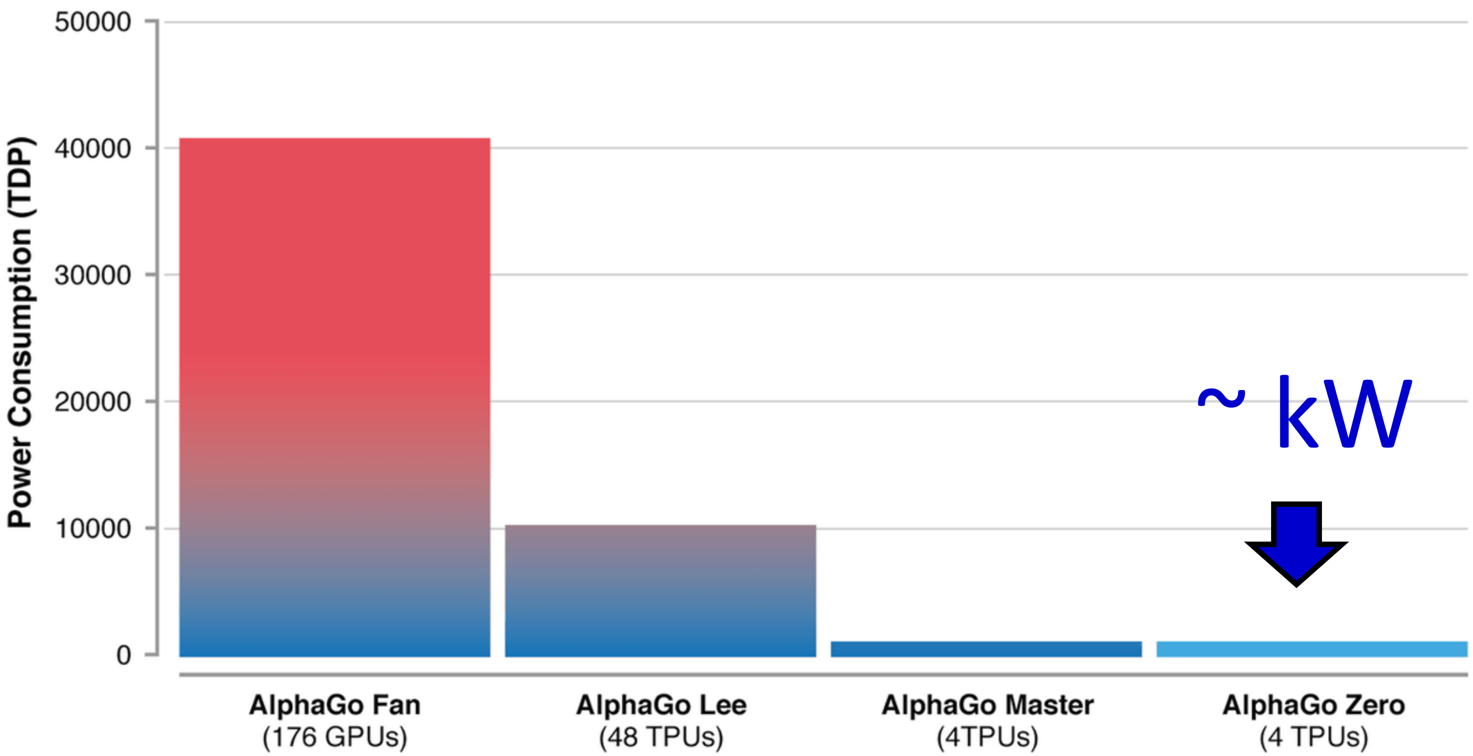
Road to neuromorphic computing (1)

Deep Neural Network (DNN) + Conventional hardware … **AI**



- Many product-sum operations
- High compatibility with conventional hardware
- Inefficient in terms of power consumption

History of AlphaGo



*TDP: Thermal Design Power

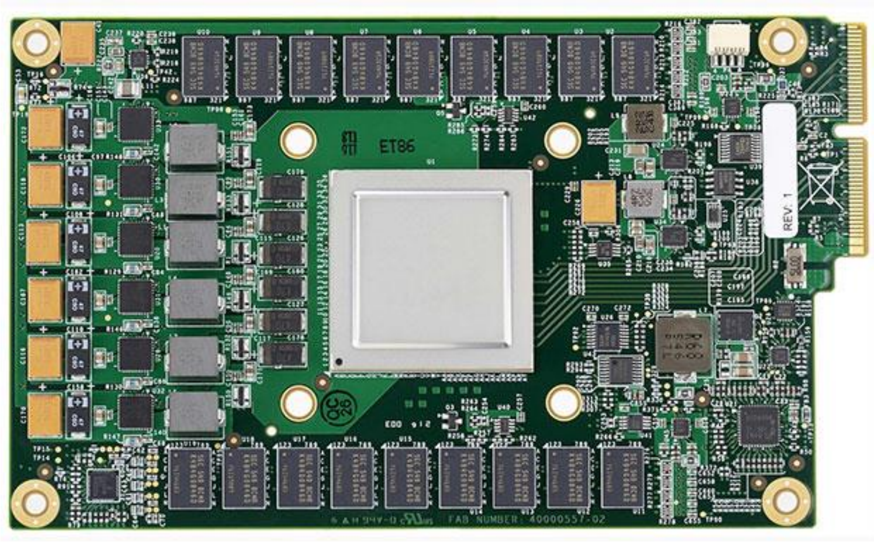
https://gigazine.net/news/20171020-alphago-zero/

- Power consumption has been drastically improved by employing **Tensor Processing Unit (TPU)**.

Road to neuromorphic computing (2)

Sophisticated architecture with CMOS (ASIC*)

Tensor Processing Unit (TPU)
by Google



Taken from IEEE Spectrum

- Specialized for product-sum operation

Other examples

TrueNorth
by IBM

BrainScaleS
by Heidelberg

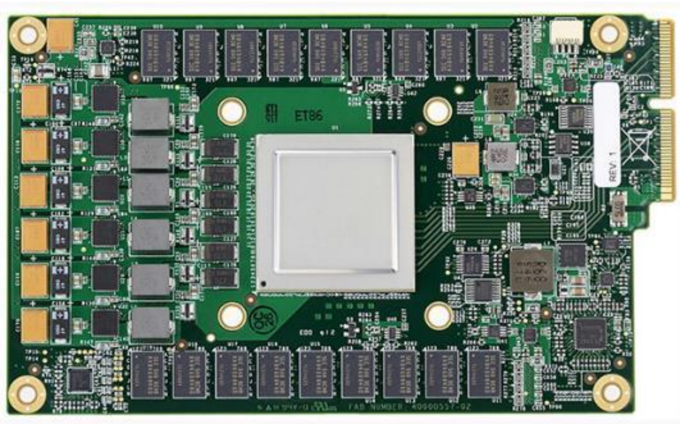
Loihi
by Intel

*ASIC: Application Specific Integrated Circuit

Road to neuromorphic computing (3)

Sophisticated architecture + **nonvolatile MTJ**

Tensor Processing Unit (TPU)
by Google

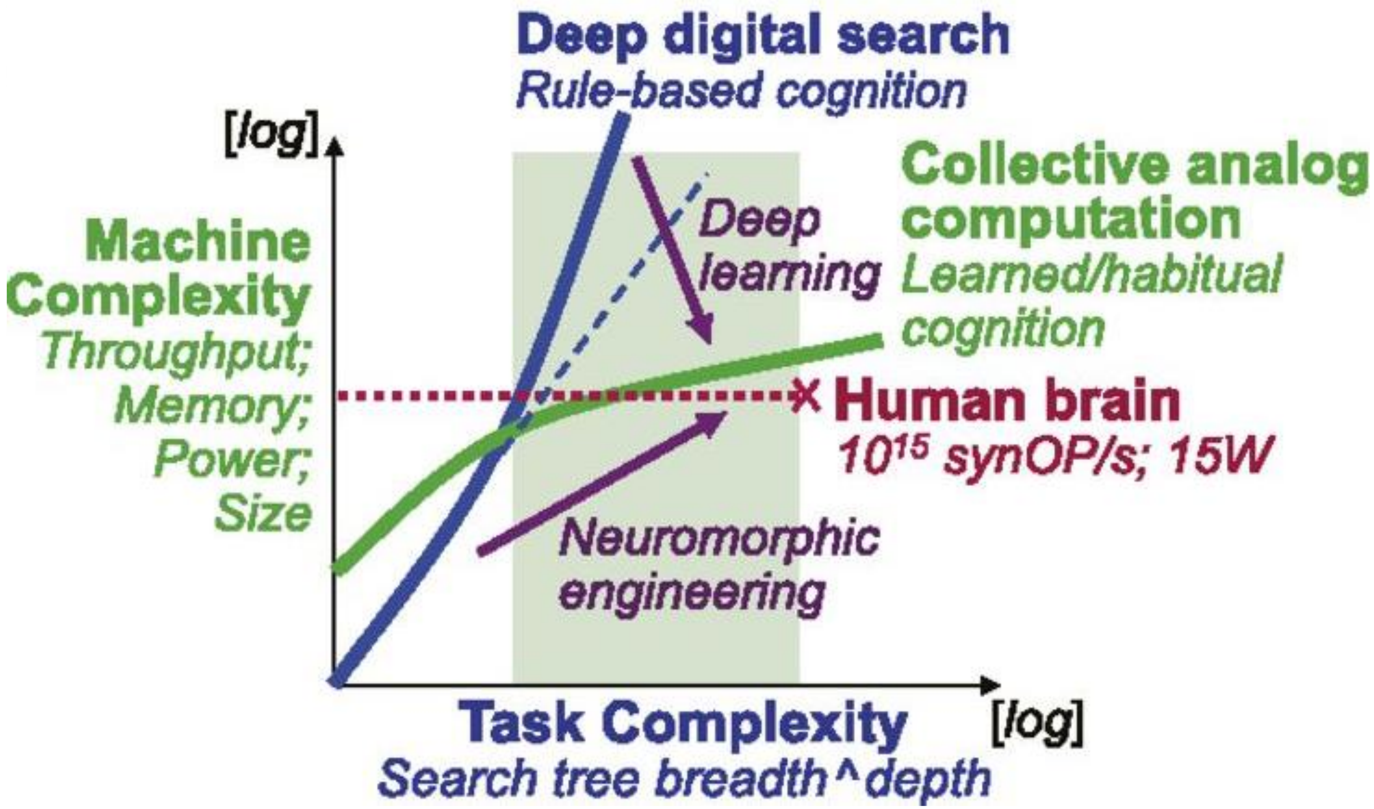


Taken from IEEE Spectrum

700 MHz
28 – 40 W
40～57 mW/MHz

* Commercially-available AI chips (2018) produced by **Gyrfalcon Technology** use TSMC's eMRAM

Scaling of machine complexity vs task complexity

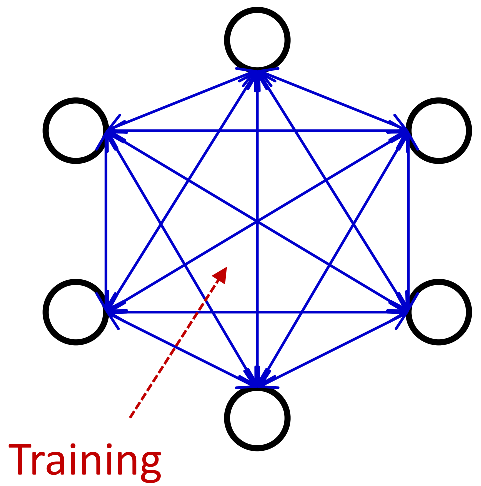


G. Cauwenberghs, PNAS **110**, 15512 (2013)

- As task complexity increases, more brain-like models with brain-like elements are promising.

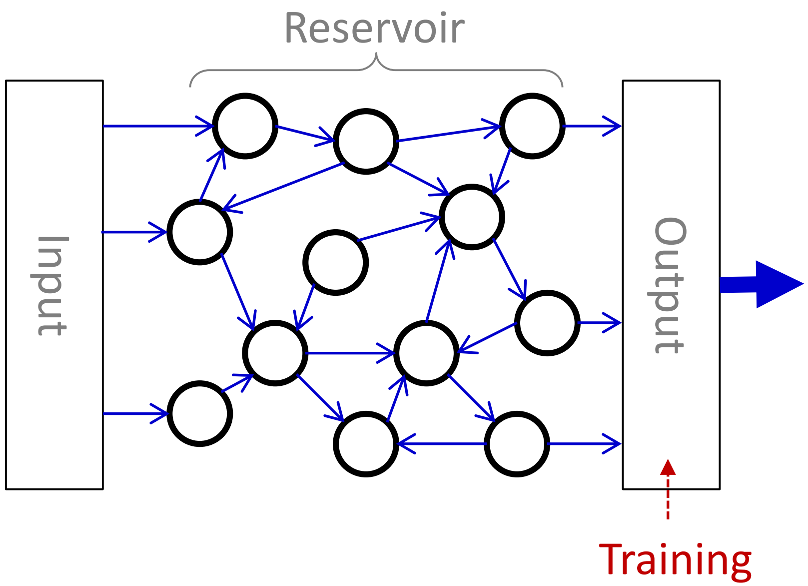
Neural network models

Hopfield model



J. J. Hopfield, *PNAS* **79**, 2554 (1982).

Reservoir computing



H. Jaeger & H. Haas, *Science*, **304**, 78 (2004)

Artificial synapse with **analog memory functionality** is required.

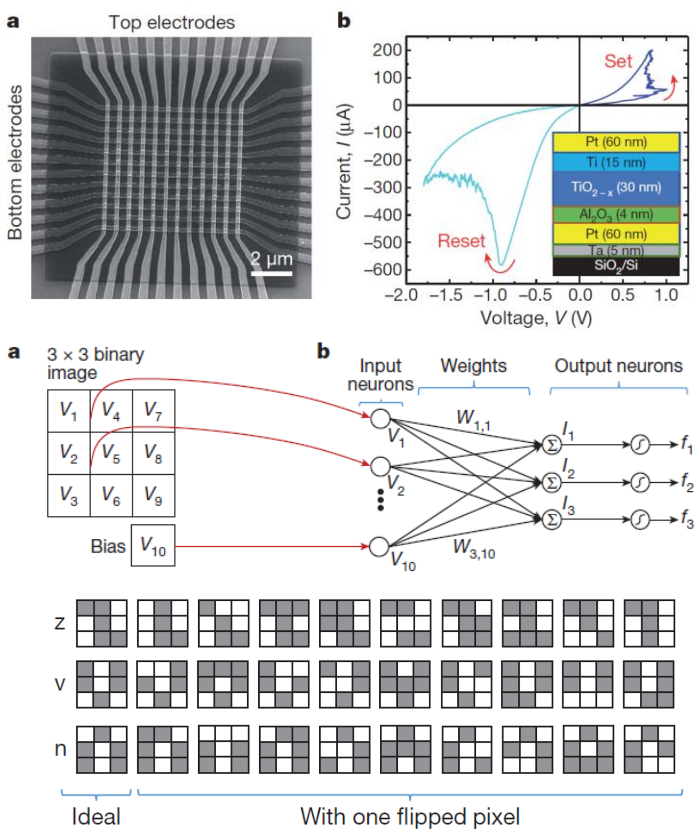
Artificial neuron with **non-linearity** and **short-term memory functionality** is required.

➔ **Emerging devices**

Road to neuromorphic computing (4)

Sophisticated architecture with emerging devices (static)

Metal-oxide memristor (TiO_{2-x})



Pattern classification using single-layer perceptron

M. Prezioso *et al.*, *Nature* **521**, 61 (2015).

Other examples

Phase-change
Hopfield network
by IBM (IEDM2013)

Ferroelectric
Hopfield network
by Panasonic
(VLSI2013)

Spintronics
Hopfield network
by Tohoku Univ.
(APEX2017)

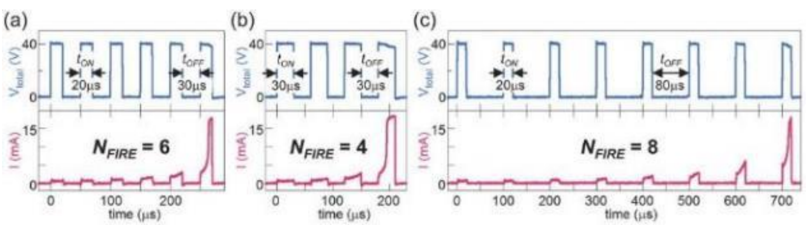
Road to neuromorphic computing (5A)

Sophisticated architecture with **emerging devices (dynamic)**

Neuron-like element

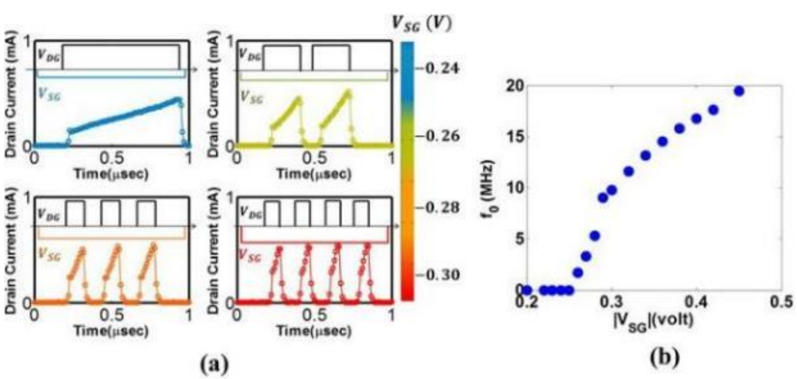
Mott Insulator

(Stoliar *et al.*, Adv. Func. Mater. 2017)



Floating-body MOSFET

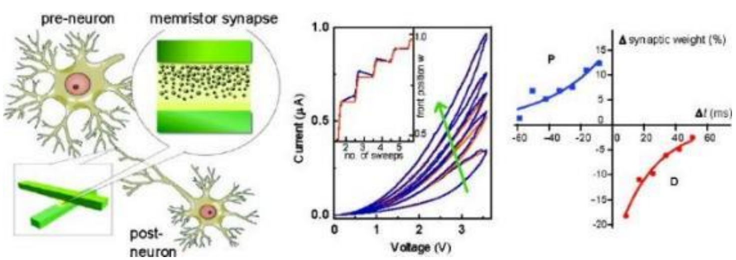
(Datta *et al.*, Sci. Rep. 2017)



Synapse-like element

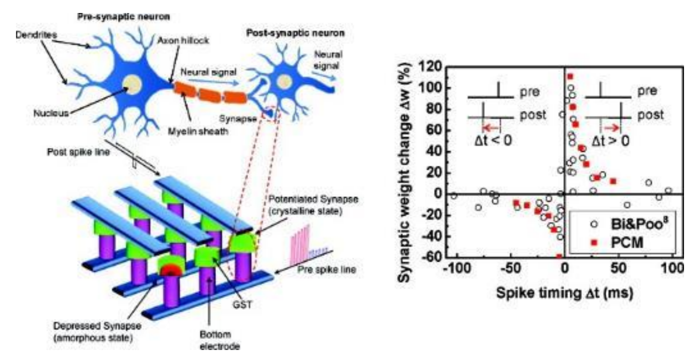
Si:Ag (memristor)

(Jo *et al.*, Nano Lett. 2010)



$Ge_2Sb_2Te_5$

(Kazum *et al.*, Nano Lett. 2012)



Spintronics … Next talk by Aleksandr Kurenkov

Road to neuromorphic computing (5B)

Sophisticated architecture with **emerging devices (dynamic)**

Reservoir computing

Water in a bucket
(C. Fernando & S. Sojakka 2003)

Memristor array
(C. Du *et al.* 2017)

Octopus
(K. Nakajima *et al.* 2013)

Example of spintronics … described later

Short summary

Status and prospect of neuromorphic computing

- Software-based approach with **conventional hardware** (So-called **AI**)
  - well established
  - requires huge power
- Sophisticated hardware (so-called **ASIC**)
  - can drastically reduce power consumption
- Sophisticated hardware + **MTJ**
  - can further reduce power consumption
- Emerging devices (neuron-like, synapse-like)
  - may have opportunities for **highly-complex tasks** … what?
  - researches on various material systems on going

… any chance for spintronics?

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Features of spintronics

TOHOKU UNIVERSITY

- High speed
  (ns ~ sub ns for FM, sub ns ~ ps for AFM)
- High endurance (>10^{15})
- Scalable (< 10 nm)
- Nonvolatile (> 10 years)
- Low voltage (< 1 V)
- Can be formed between interconnect

MRAM

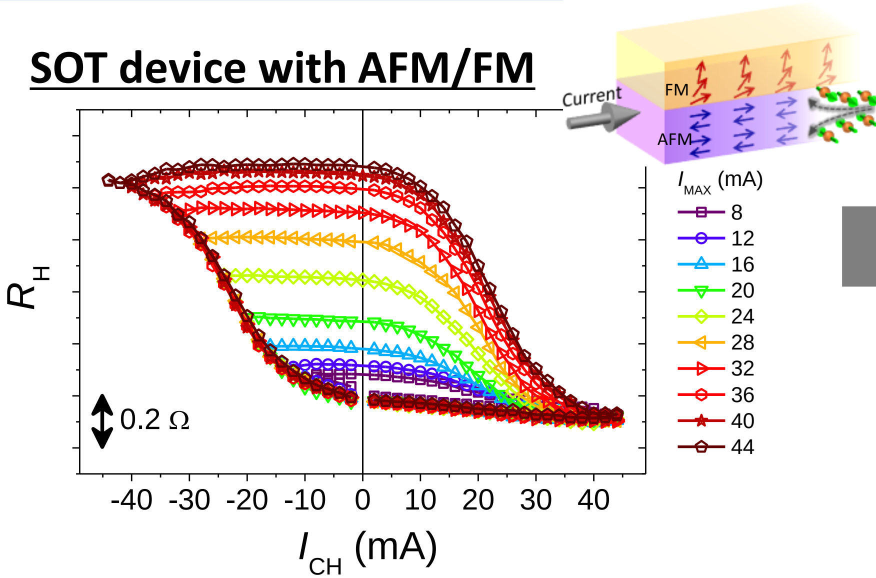
- **Analog/digital mixed**
- **Short-term memory**
- **Stochasticity**

Neuro-morphic

- [Cons] Low magnetoresistance → needs to be helped by CMOS

Example 1) Analog memory functionality

SOT device with AFM/FM



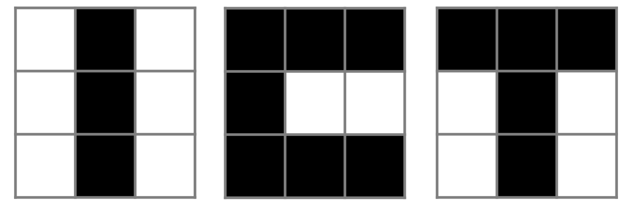
S. Fukami *et al.*, Nature Mater. **15**, 535 (2016).
Poster by G. Krishnaswamy, SF *et al.*

- Controlling domain structure allows analog memory.

Similar behavior:

- **CuMnAs** … P. Wadley *et al.*, Science (2016); K. Olejnik *et al.*, NCOMMS (2017).
- **Mn_2Au** … S. Y. Bodnar *et al.*, NCOMMS (2018); M. Mainert *et al.*, PRAppl (2018).
- **NiO** … X. Z. Chen *et al.*, PRL (2018); T. Moriyama *et al.*, SciRep (2018).

Associative memory

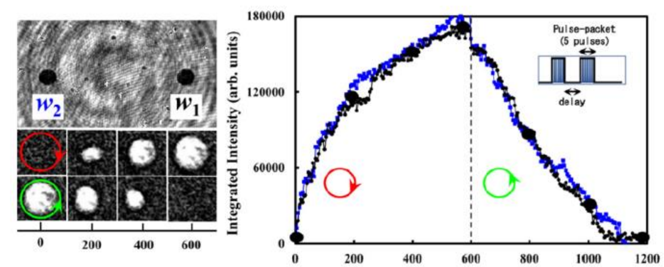


W. A. Borders, SF *et al.*, Appl. Phys. Express **10**, 013007 (2017).

- 36 analog SOT devices used as artificial synapse in Hopfield network.

Another example

Helicity-dependent optical switching in Co/Pt

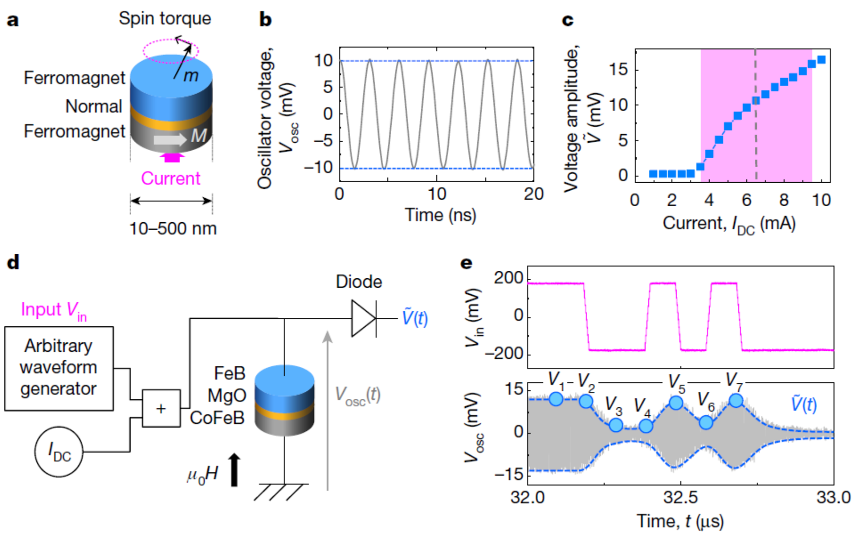


Supervised perceptron leaning demonstrated

A. Chakravarty *et al.*, *APL* (2019)

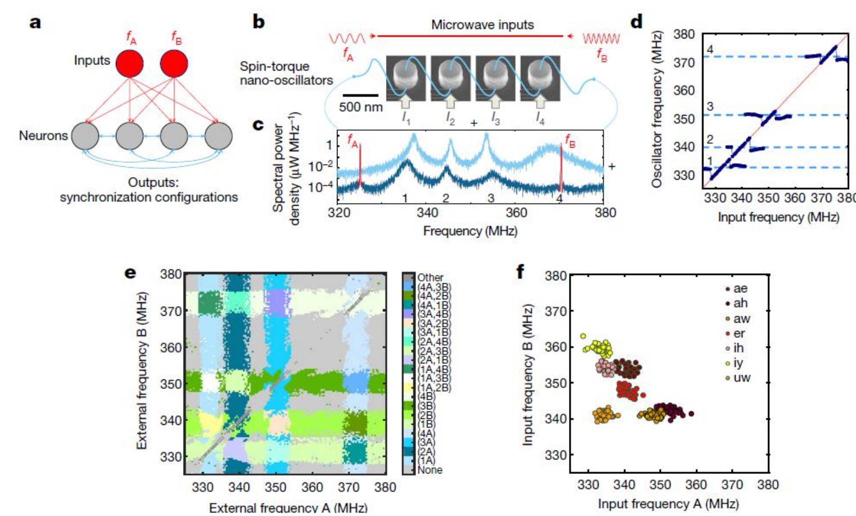
Example 2) Short-term memory functionality

Spoken digit recognition



J. Torrejon *et al.*, Nature **547**, 428 (2017)

Vowel recognition



M. Romera *et al.*, Nature **563**, 230 (2018).

Also, …

- Synchronization functionality of STO is useful for pattern matching.

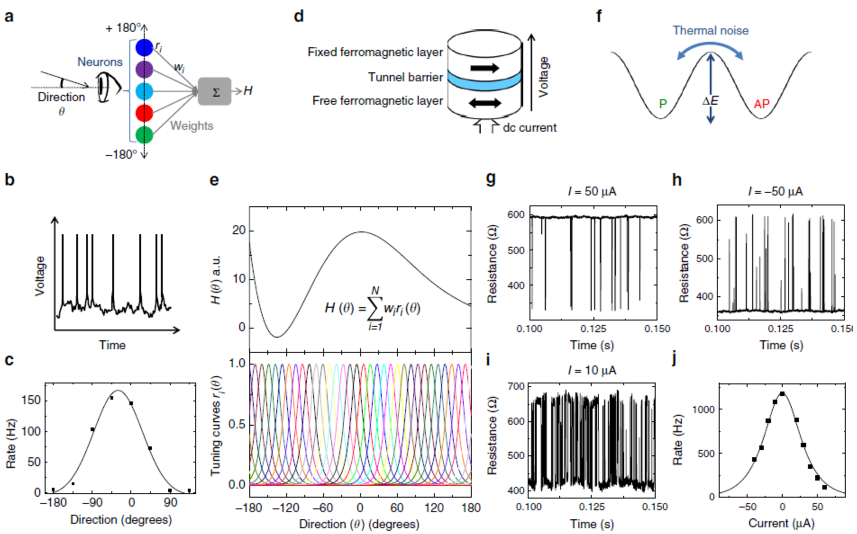
  M. R. Pufall *et al.*, IEEE J. Explor. Solid-State Comput. Dev. Cir. **1**, 76 (2015).

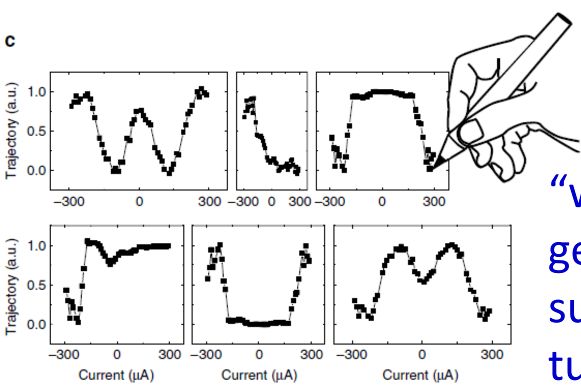
- Skyrmion fabrics, spin wave in garnet, … can be used for reservoir layer.

  D. Prychynenko *et al.*, Phys. Rev. Appl. **9**, 014034 (2018).
  R. Nakane *et al.*, IEEE Access **6**, 4462 (2018).

Example 3) Stochasticity

Population coding

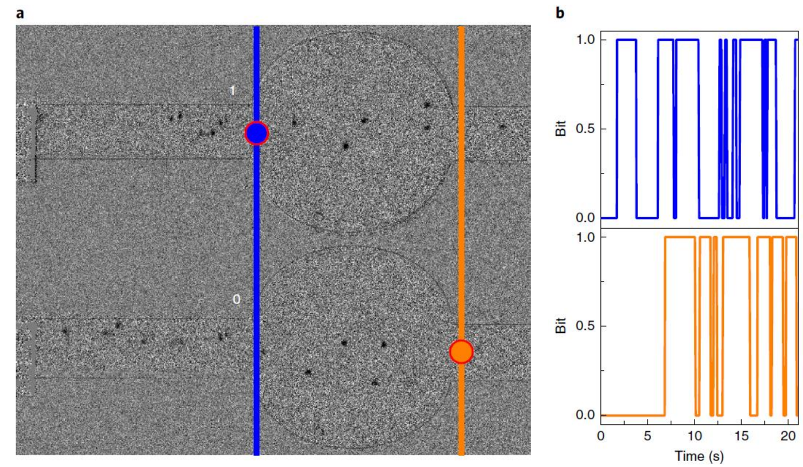




“w, i, n, r, u, m” generated by superparamagnetic tunnel junction

A. Mizrahi *et al.*, NCOMMS **9**, 1533 (2018).

Stochastic computing



Brownian motion of skyrmion to generate uncorrelated random bit

J. Zázvorka *et al.*, NNANO **14**, 658 (2019).

Probabilistic computing ... described later

Challenges and opportunities of spintronics
(my thought)

- Spintronics is attractive in terms of rich attributes (**analog**, **dynamics**, **stochastic**, ...) and controllability.
- **Small-scale proof-of-concept demonstration** has been going well.
- **Large-scale performance demonstration** compared with competing technologies will be demanded in future.
- Need to be conscious of **integration into CMOS** circuits.
- Need to find applications that are difficult for other technologies.

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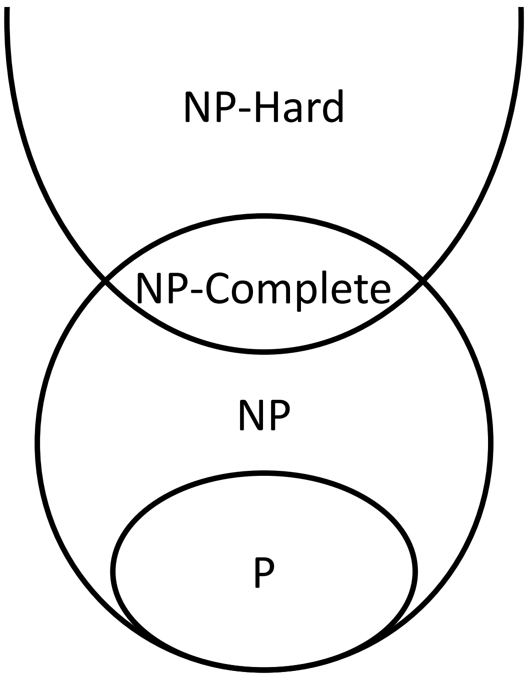
Computational complexity



Class P

Problems that can be solved by a deterministic Turing machine using a polynomial time.

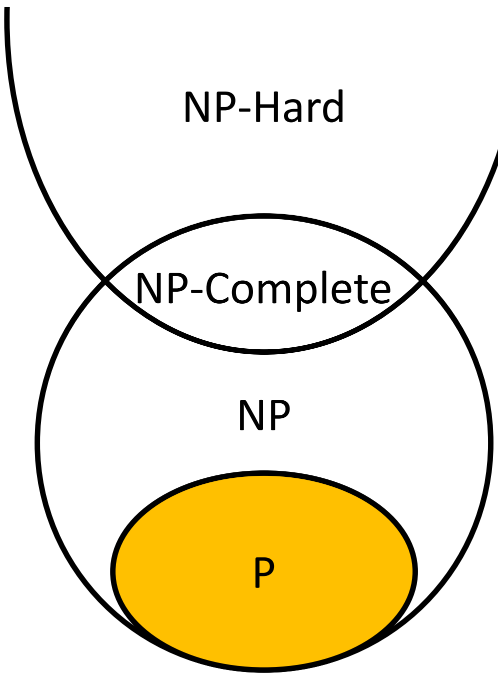
Class NP

Problems where the validity of answer can be verified with polynomial time.

Class NP-Hard

Problems that are informally "at least as hard as the hardest problems in NP".

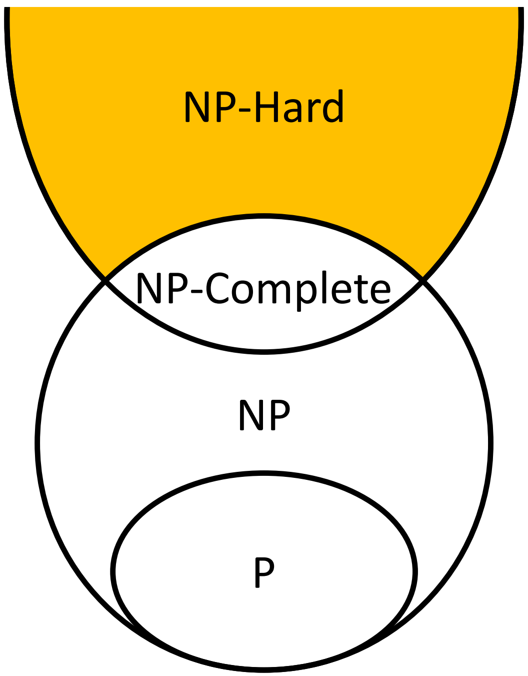
Problem 1) Class P



Q. You will travel the cities below.
How long does it take?

1. Frankfurt
2. Munich
3. Roma
4. Milano
5. Marseille
6. Barcelona
7. Madrid
8. Paris
9. London
10. Amsterdam
11. Stockholm
12. Warsaw
13. Frankfurt

Problem 2) Class NP-Hard



Q. You are at Frankfurt. You should visit the cities below once and return to Frankfurt. What's the shortest route?

- Munich
- Roma
- Milano
- Marseille
- Amsterdam
- Stockholm
- Warsaw

Traveling Salesman Problem

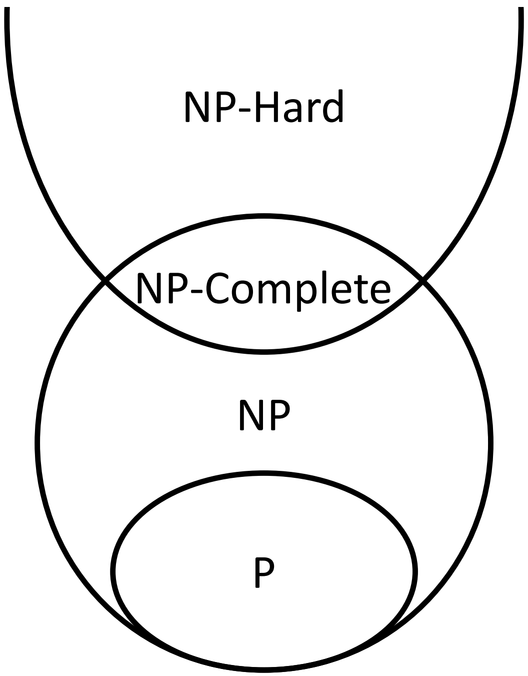
(Optimization problem)

30 cities → 4.42×10^{30} patterns → 10^{13} years !!! by high-performance computer

(Lifetime of sun … 10^{9} years)

Integer factorization

35 = 5 x 7
161 = 23 x 7

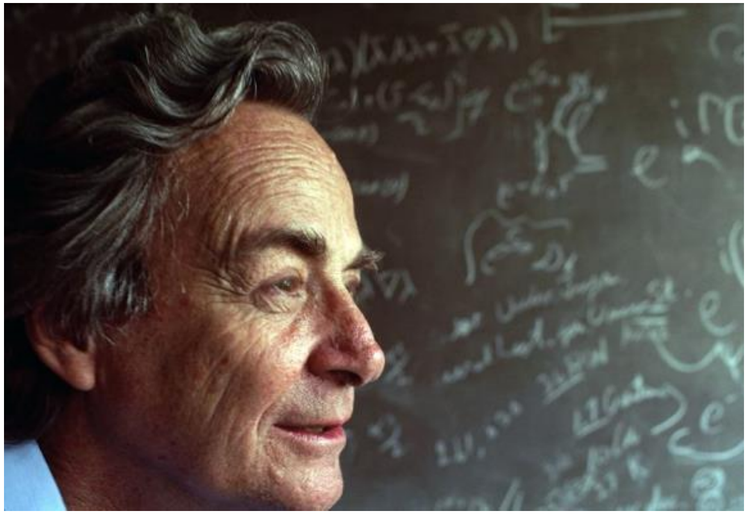


- Belong to Class NP(-hard) (controversial)
- Very difficult for classical computers
  - State-of-the-art computer at 2007 took 2.5 years to factorize 768 bit.
    T. Kleinjung *et al.*, Advances in Cryptology – CRYPTO 2010 p. 333 (2010)
- Applied to data encryption
- Known to be efficiently solved by quantum computer (Shor's algorithm)

Other examples in difficult-class problem:
- Calculation of wave function of molecules, weather forecast, …

Richard Feynman said …

"Simulating Physics with Computers"



https://www.nature.com/articles/d41586-019-02781-4

Physics of Computation Conference
at MIT
on May 6-8, 1981

"If you want to make a simulation of nature, you'd better make it quantum mechanical, …"

Quantum computing

"…the other way to simulate a probabilistic nature is by a computer which itself is probabilistic, …"

Probabilistic computing

"Simulating Physics with Computers", International Journal of Theoretical Physics **21**, 467-488 (1982).

Probabilistic computing – basic concept

$$P(E,T) = \frac{1}{Z}\exp\left[-\frac{E(\Gamma)}{k_{\mathrm{B}}T}\right]$$

… Boltzmann distribution

The lowest energy state is most-frequently observed.

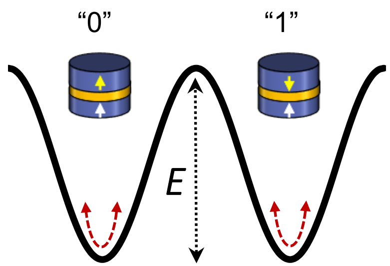
(The lowest energy state is observed at $T \rightarrow 0$ ➔ Annealing)

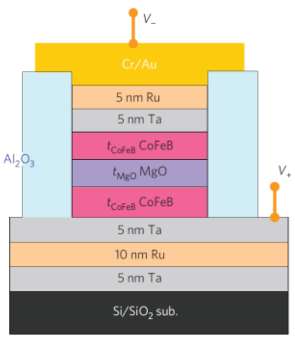
Procedure of probabilistic computing

1. Defining **energy (cost function)** for the given problem.
2. Mapping to **physical system with probabilistic nature**.
3. Taking **statistics** of stochastic neurons.
4. You will obtain the answer as the state **that had been observed most frequently**.

Stochastic magnetic tunnel junction

MRAM

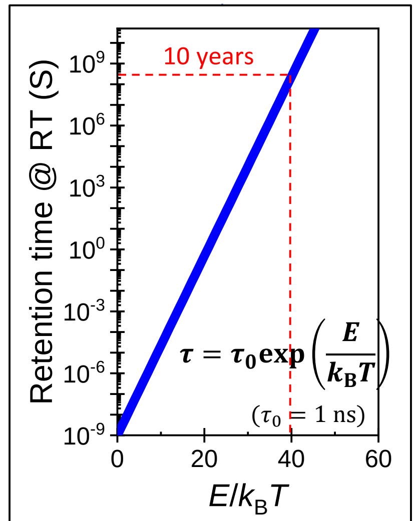




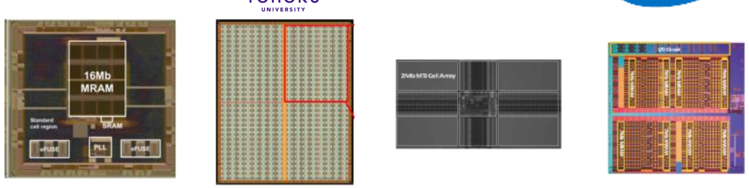
$$\frac{E}{k_B T} = 40$$

@ t_{CoFeB} =1.7 nm

S. Ikeda *et al.*, NMAT **9**, 721 (2010)



W. F. Brown, Phys. Rev. **130**, 1677 (1963).



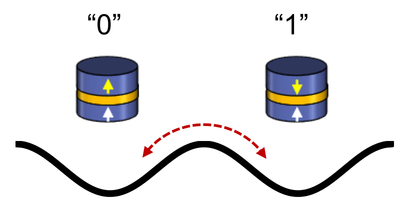
16 Mb. VLSI2018

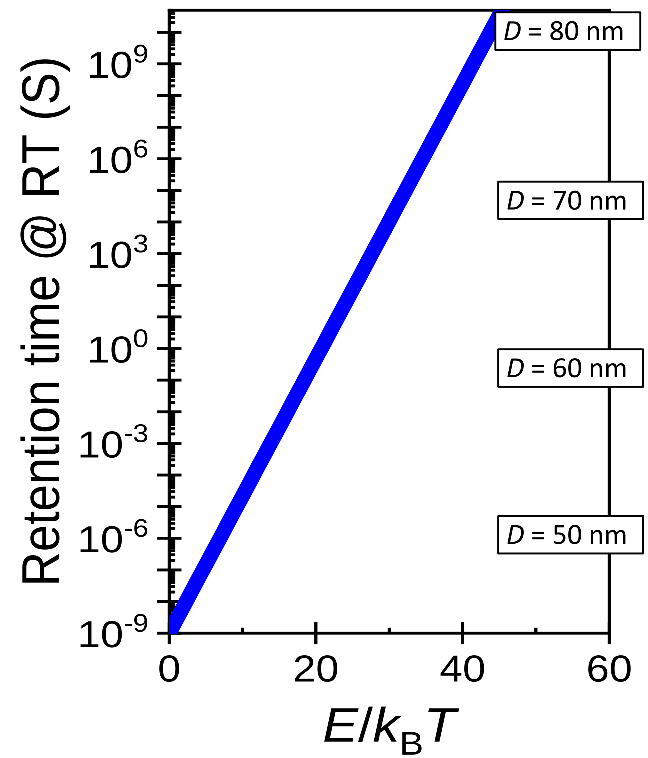
128 Mb. IEDM2018

8 Mb. IEDM2018

7 Mb. ISSCC2019

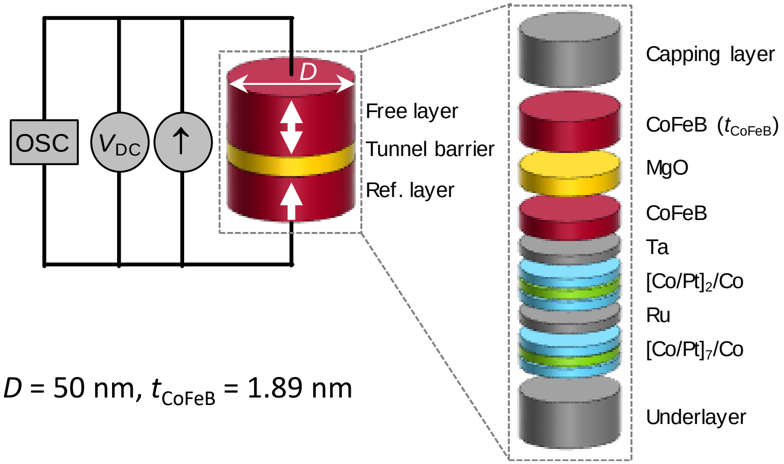
Probabilistic bit (p-bit)





W. A. Borders *et al.*, Nature **573**, 390 (2019).

Spintronics p-bit

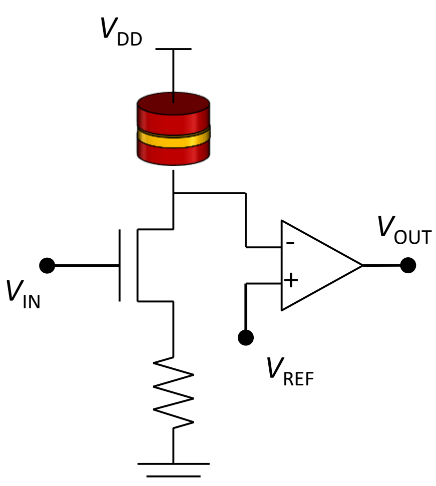


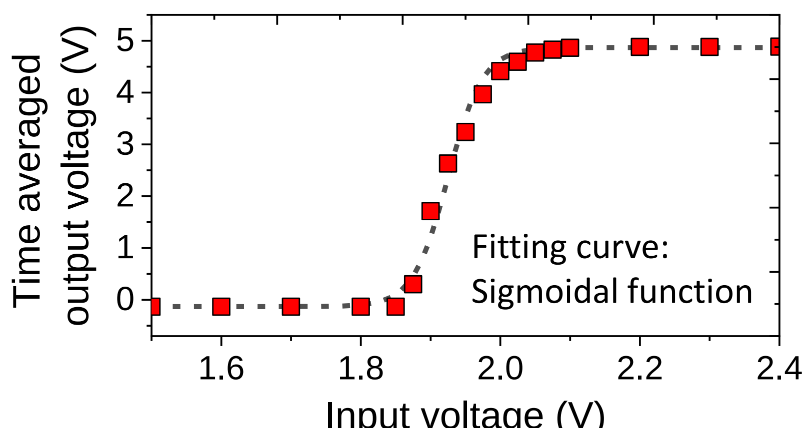
D = 50 nm, t_{CoFeB} = 1.89 nm

I = -13.0 μA

I = -11.0 μA

I = -9.0 μA





Stochastic neuron!

K. Y. Camsari *et al.*, IEEE Elec. Dev. Lett. **38**, 1767 (2007).

Used algorithm for integer factorization

$$E = (XY - F)^2$$

Optimum combination of
X and *Y* that minimize *E*
(Optimization problem)

$$\begin{cases} X = 1 + 2x_1 + 4x_2 + 8x_3 + \cdots \\ Y = 1 + 2y_1 + 4y_2 + 8y_3 + \cdots \end{cases}$$

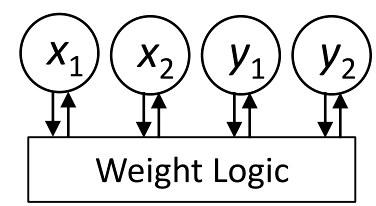
- **Example) Factorizing 35 (= *F*) by 4 bits (x_1, x_2, y_1, y_2)**

coefficients are rounded off to have one significant digit.

$$E = -0.3x_1 - 0.7x_2 - 0.3y_1 - 0.7y_2 - x_2y_1 - 1.4x_2y_2 - 0.6x_1y_1$$
$$-x_1y_2 + 0.3\underline{x_1y_1y_2} + \underline{x_2y_1y_2} + 0.3\underline{x_1x_2y_1} + \underline{x_1x_2y_2} + 0.7\underline{x_1x_2y_1y_2}$$

3-body interaction 4-body interaction

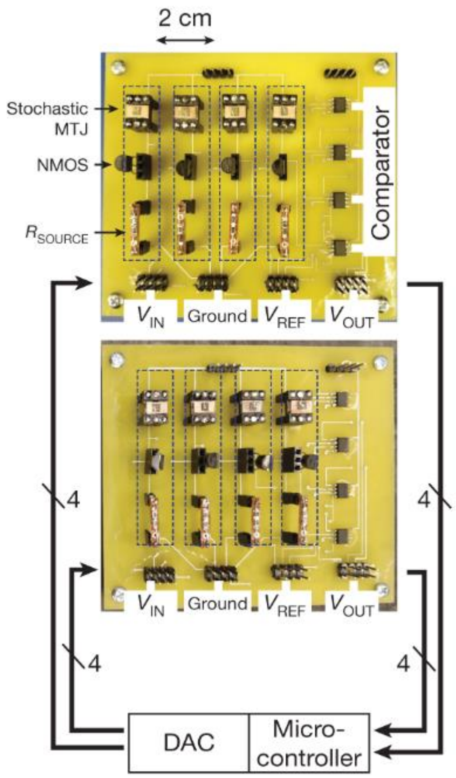
$$\begin{cases} I_{x1} = -\dfrac{\partial E}{\partial x_1} = 0.3 + 0.6y_1 + 1.0y_2 - 0.3y_1y_2 - 0.3x_2y_1 - 1.0x_2y_2 - 0.7y_1x_2y_2 \\ I_{x2} = -\dfrac{\partial E}{\partial x_2} = 0.7 + 1.0y_1 + 1.4y_2 - 1.0y_1y_2 - 0.3x_1y_1 - 1.0x_1y_2 - 0.7x_1y_1y_2 \\ I_{y1} = -\dfrac{\partial E}{\partial y_1} = 0.3 + 0.6x_1 + 1.0x_2 - 0.3x_1y_2 - 1.0x_2y_2 - 0.3x_1x_2 - 0.7x_1x_2y_2 \\ I_{y2} = -\dfrac{\partial E}{\partial y_2} = 0.7 + 1.0x_1 + 1.4x_2 - 0.3y_1x_1 - 1.0y_1x_2 - 1.0x_1x_2 - 0.7x_1x_2y_1 \end{cases}$$



W. A. Borders *et al.*, Nature **573**, 390 (2019).

Result of integer factorization

$F = 35$ $F = 161$ $F = 945$



Points

- Possible to operate at **room temperature**
- Based on **Mb-level** of STT-MRAM technology
- Easy to implement **many-body interaction**
- Small

Outline

0. Preface
1. General introduction to neuromorphic computing
2. Status and prospect of spintronics
3. Recent example: probabilistic computing using stochastic magnetic tunnel junction
4. Conclusion

● Announcement #1

http://www.spin.riec.tohoku.ac.jp/17thRIEC/index.html

Topics

Antiferromagnetic spintronics,
Spin-orbitronics,
Unconventional computing

Special Lecturers

Irina Kataeva (DENSO Corp.)
"Tutorial on neuro-computing for automotive applications"

Masayuki Ohzeki (Tohoku University)
"Tutorial on Quantum Annealing"

Free of charge

Submit an abstract for poster presentation

Confirmed Invited Speakers

Johan Åkerman (Gothenburg)
Martin Aeschlimann (Kaiserslautern)
Jingsheng Chen (Singapore)
Tomasz Dietl (Warsaw)
Atsufumi Hirohata (York)
Aleš Hrabec (Zürich)
Stéphane Mangin (Lorraine)
Keith McKenna (York)
Shigemi Mizukami (Tohoku)
Yuriy Mokrousov (Jülich)
Teruo Ono (Kyoto)
Yoshichika Otani (Tokyo)
Daniele Pinna (Mainz)
Philipp Pirro (Kaiserslautern)
Günter Reiss (Bielefeld)
Eiji Saitoh (Tohoku/Tokyo)
Takeshi Seki (Tohoku)
Masafumi Shirai (Tohoku)
Mark Stiles (NIST)
Yoshishige Suzuki (Osaka)
Rie Umetsu (Tohoku)
Seonghoon Woo (IBM)
Jörg Wunderlich (Cambridge)

Announcement #2

JAP Special Topic: Antiferromagnetic Spintronics

This Special Topic includes - but is not limited to - the following areas:
- Electrical or optomagnetic control of antiferromagnets
- Spin-orbit interactions and torques
- Ultrafast spin dynamics
- Antiferromagnetic textures: Domain walls, skyrmions, etc.
- Spin waves
- Characterization and imaging of antiferromagnets
- Microfabrication and thin film deposition techniques
- Spin transport properties including spin hall effect, spin galvanic effect, etc.
- Topological Hall effect
- Chiral anomaly
- Controlled exchange coupling
- Interaction with topologically protected electronic states
- Calculations of magnetic structure
- Insulating and metallic antiferromagnets
- Collinear vs noncollinear antiferromagnets
- Antiferromagnet/ferromagnet interfaces
- Synthetic antiferromagnets
- Memory devices
- Neuromorphic/brain-inspired computing

Submission Deadline: February 28, 2020

Guest Editors

Virginia O. Lorenz
(University of Illinois at Urbana-Champaign)

Shunsuke Fukami
(Tohoku University)

Olena Gomonay
(Johannes Gutenberg University Mainz)

Take-home messages

TOHOKU UNIVERSITY

- Classical computing hardware is inefficient for complex tasks.
- Employing brain-like architecture and nonvolatile memory drastically reduce power consumption.
- Employing emerging devices may have a chance for further complex tasks. But what are they?
- Spintronics is attractive. But, competitive?
- Spintronics p-bit is promising for optimization problems.

W. A. Borders *et al.*, Nature **573**, 390 (2019).

Review paper:

1. S. Fukami and H. Ohno, "Perspective: Spintronic synapse for artificial neural network," *J. Appl. Phys.* **124**, 151904 (2018).
2. J. Grollier, D. Querlioz, K. Y. Camsari, K. Everschor-Sitte, S. Fukami, M. D. Stiles "Neuromorphic spintronics" to be published in *Nature Electronics* (2019).