ETH zürich

Magnetic tunnel junctions and magnetic logic circuits driven by spin-orbit torques

P. Gambardella

Department of Materials, ETH Zürich, Switzerland

E. Grimaldi
V. Krizakova
P. Dao
A. Hrabec
M. Wörnle
S. Velez

K. Garello
F. Yasin
S. Couet
G.S. Kar

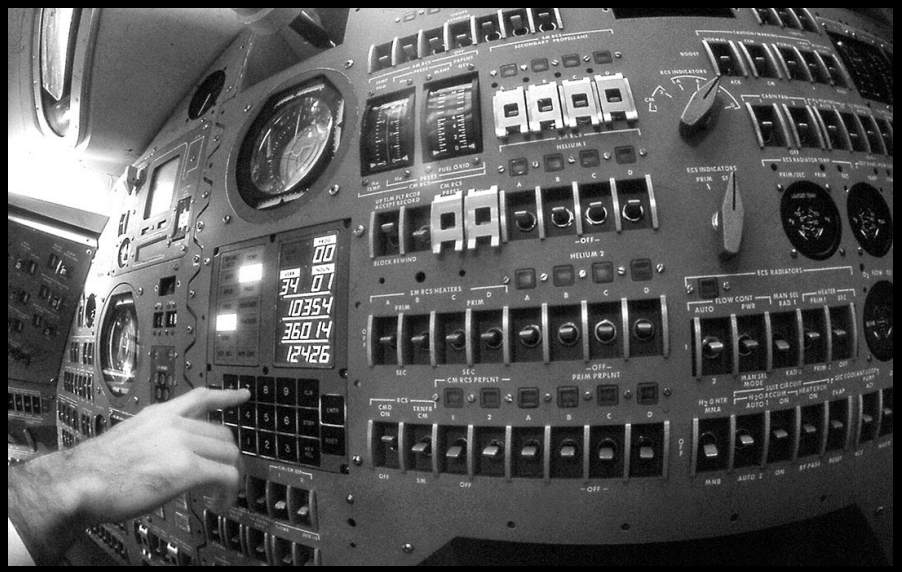
Z. Luo
A. Hrabec
A. Kleibert
L. Heyderman

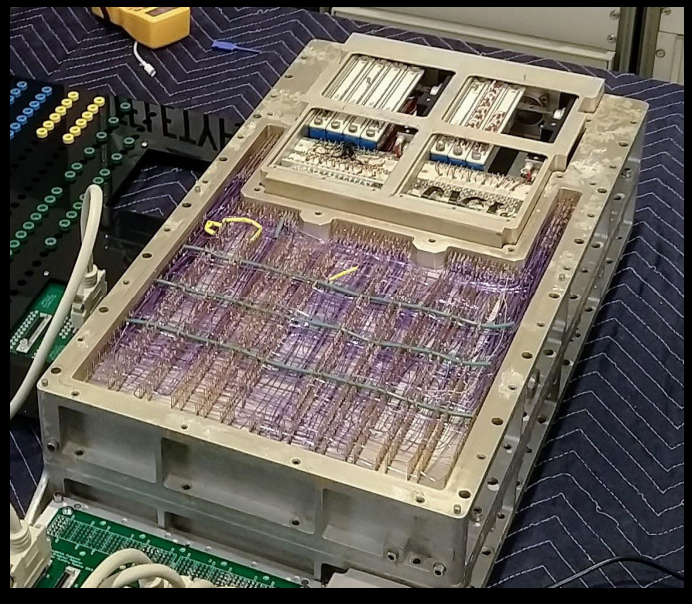
ETH Zürich imec PSI

FNSNF


USA

The Apollo Guidance Computer

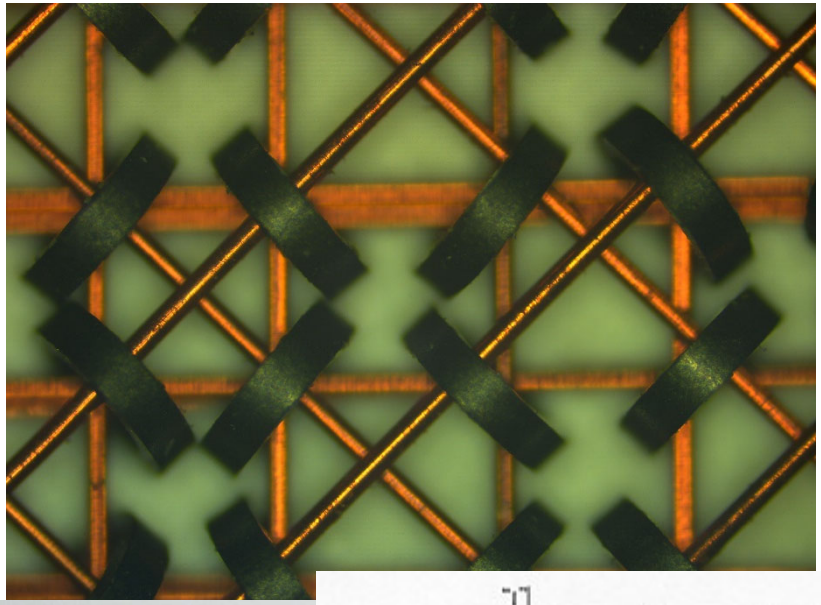


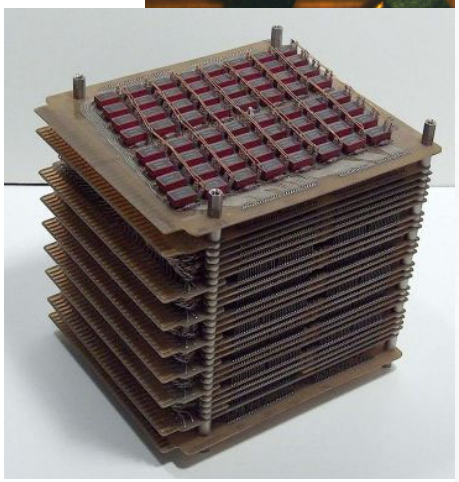


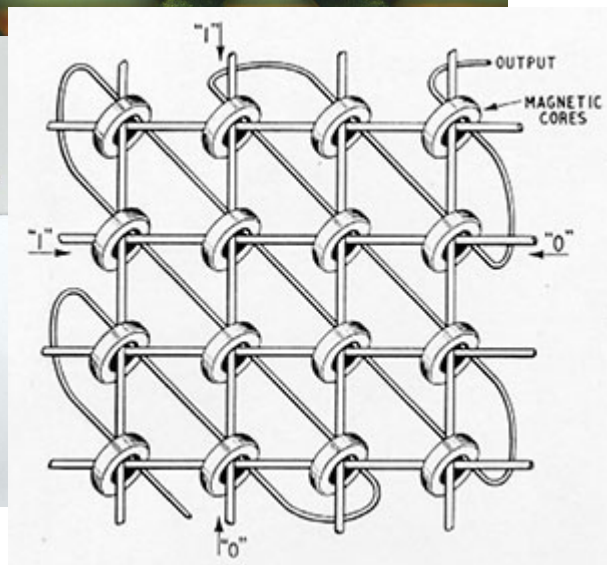
Images from NASA and Wikipedia

The magnetic core memory

Magnetic-core memory was the predominant form of random-access computer memory between 1955 and 1975. It was used in the Apollo Guidance Computer and Space Shuttle IBM flight computers until 1990.

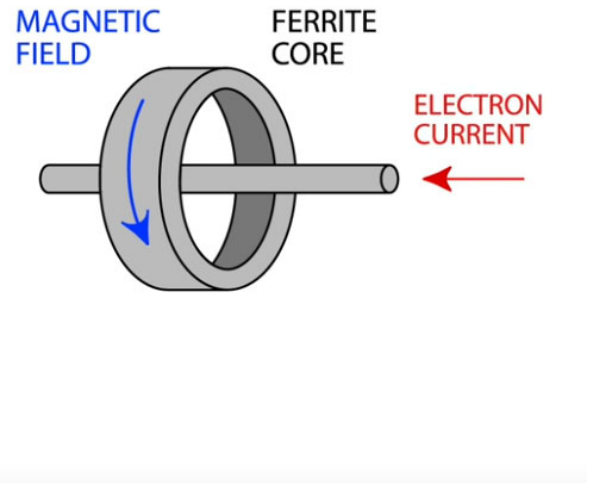


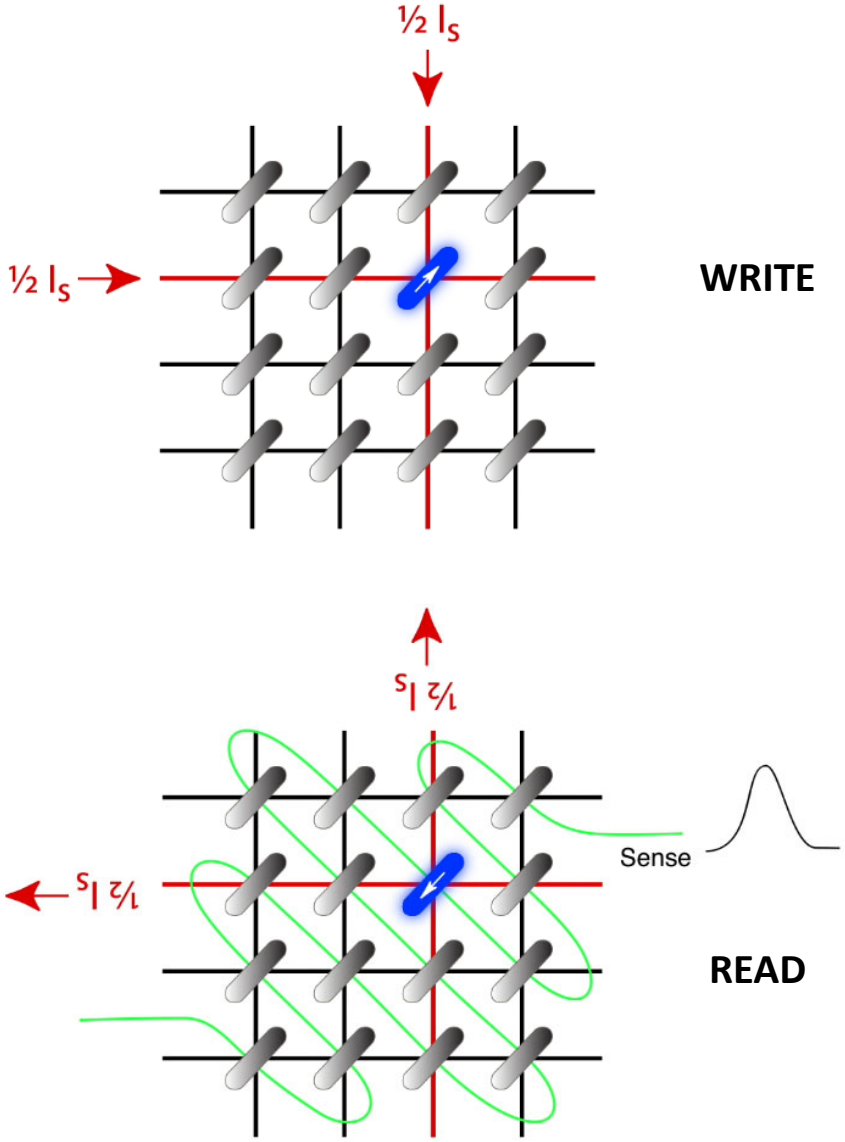




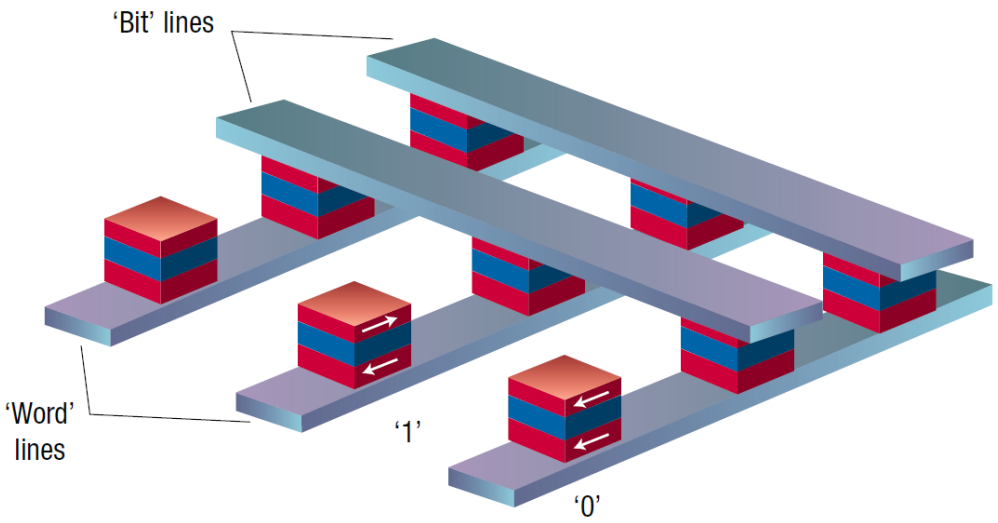
- Non-volatile
- Clock rate of ~1 MHz.
- 32 kilobits per cubic foot
- 1 cent per bit.

The magnetic core memory



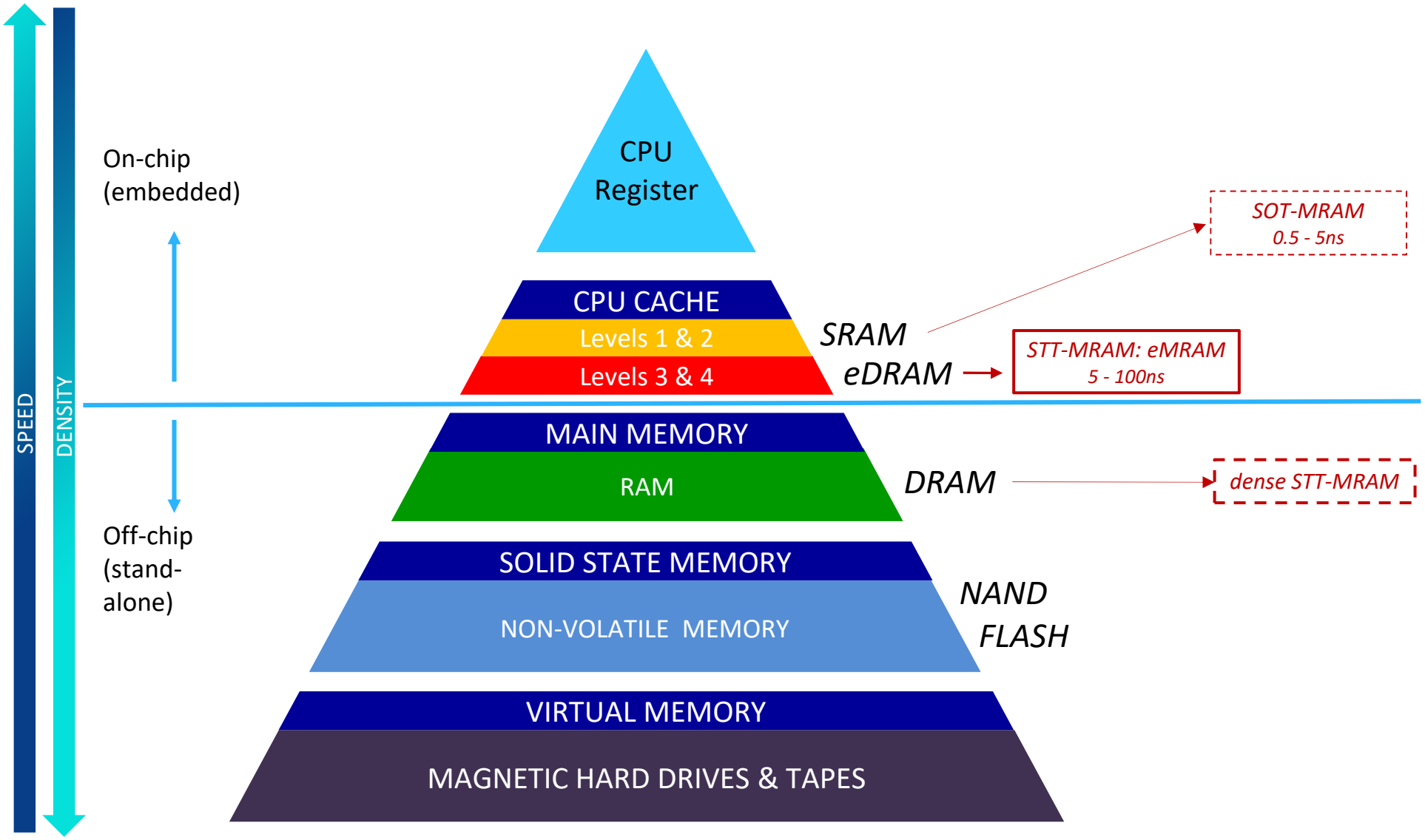


A modern magnetic random access memory

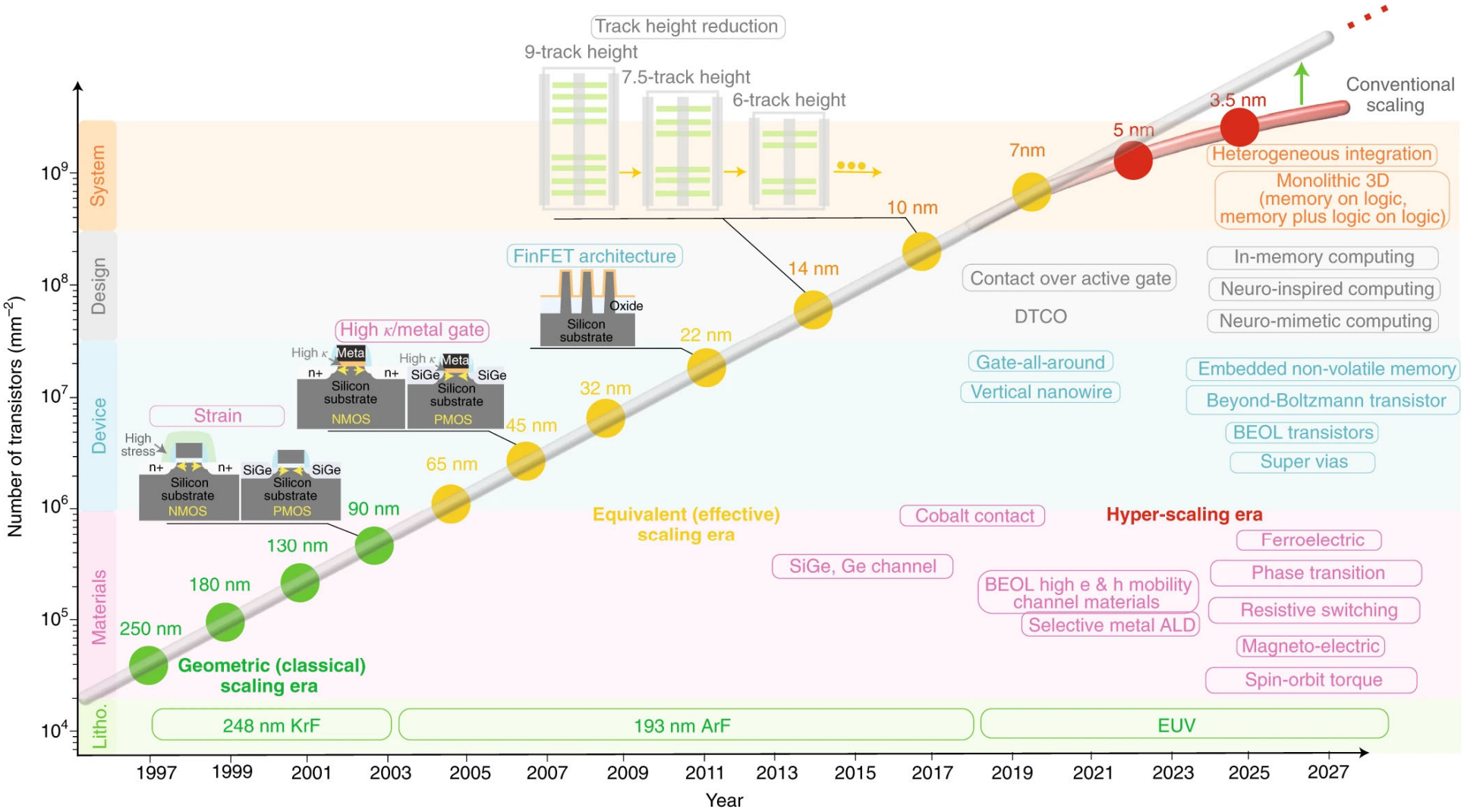


Chappert, Fert & Van Dau, Nat. Mater. 2007

Need for fast & nonvolatile memories

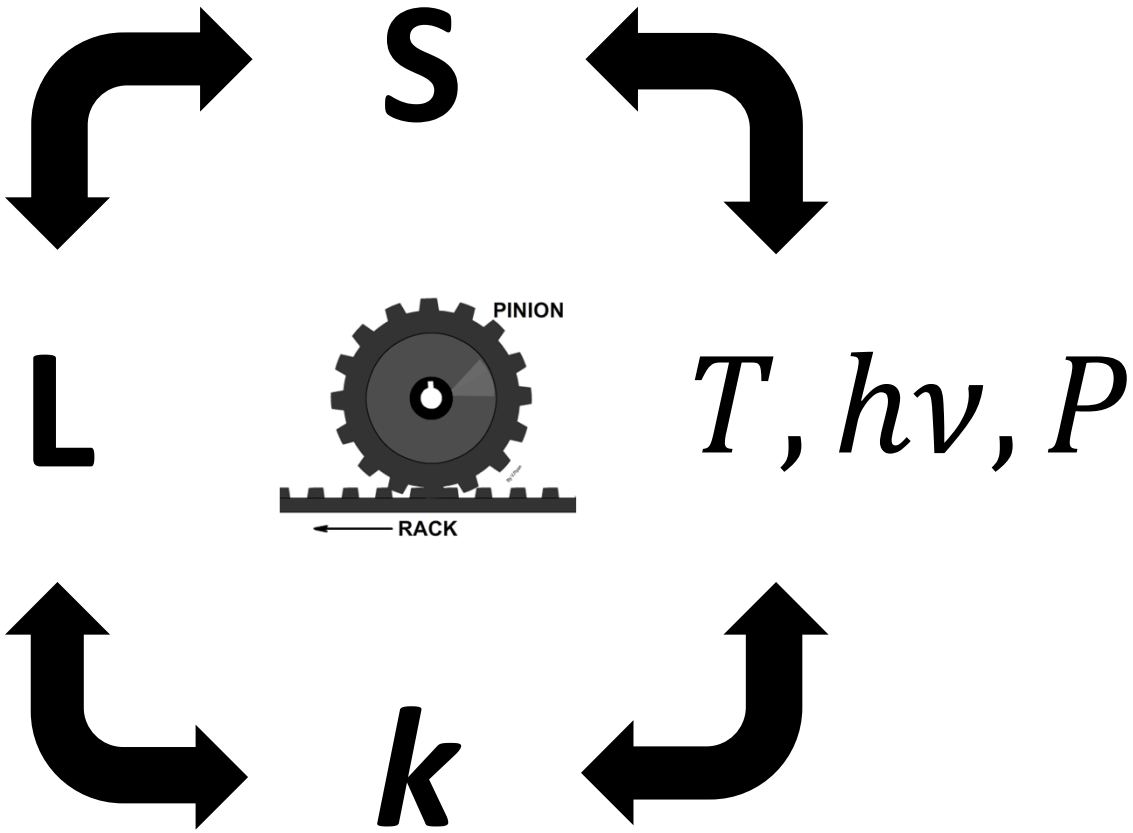


Beyond-CMOS electronics

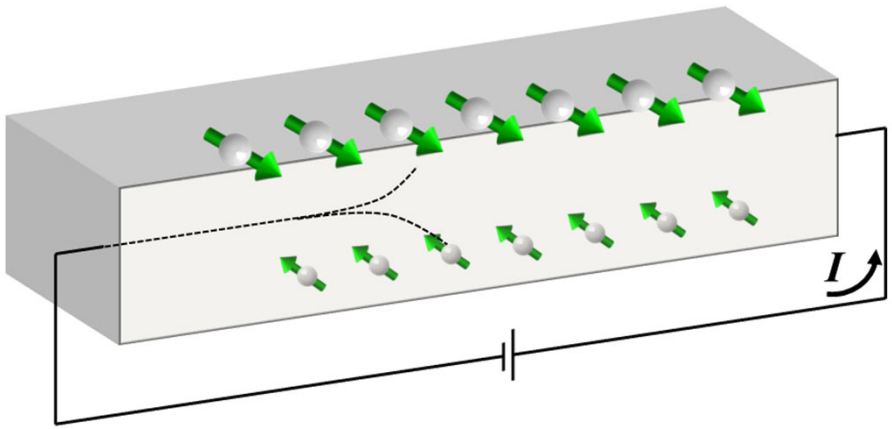


Salahuddin and Datta, Nat. Electr. **1**, 442 (2018)

Interconversion of linear momentum, angular momentum & …



The spin Hall effect



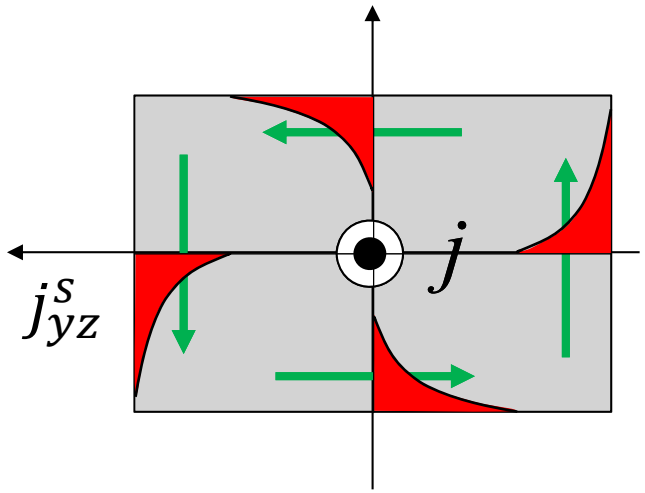
Dyakonov and Perel, JETP Lett. **13**, 467 (1971)

Kato et al., Science **306**, 1910 (2004)

Wunderlich, Phys. Rev. Lett. **94**, 047204 (2005)

Sinova et al., Rev. Mod. Phys. **87**, 1213 (2015)

$$j_{zy}^{s} = \theta_{SH}\, j_{x}^{c}$$

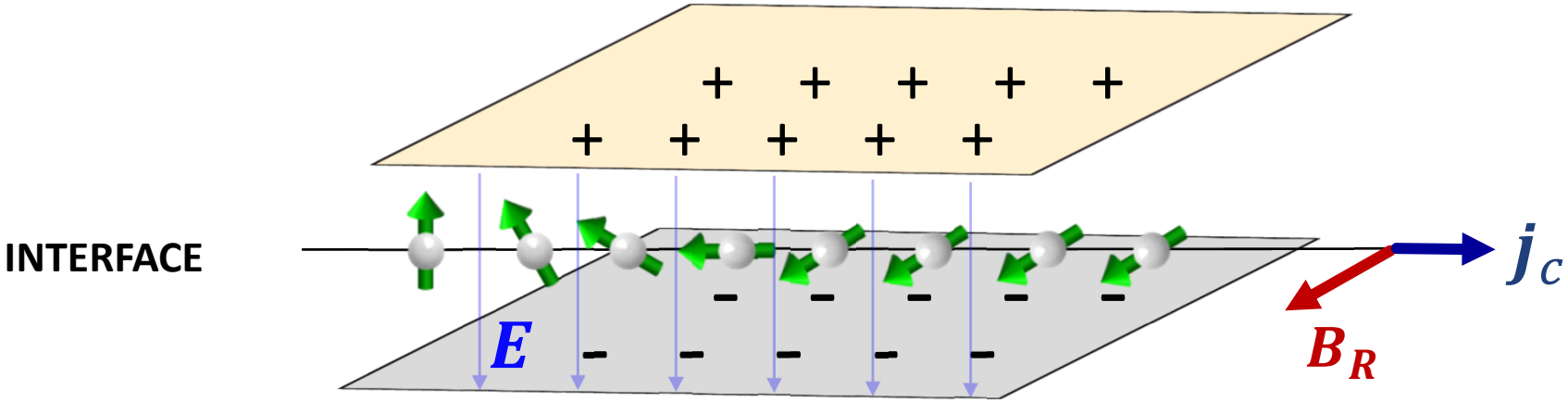


$$\theta_{SH} = \frac{j_s}{j_c} = \frac{\sigma_{yx}^{SH}}{\sigma_{xx}}$$

$$\theta_{SH}(\mathrm{Pt}) = 0.05 - 0.2$$

$$\lambda_s(\mathrm{Pt}) = 1 - 14\ nm$$

The Rashba-Edelstein effect



Electrons move in an uncompensated $\boldsymbol{E}$-field: $\boldsymbol{B_R} \sim \boldsymbol{v} \times \boldsymbol{E} \sim \boldsymbol{j_c} \times \hat{\boldsymbol{z}}$

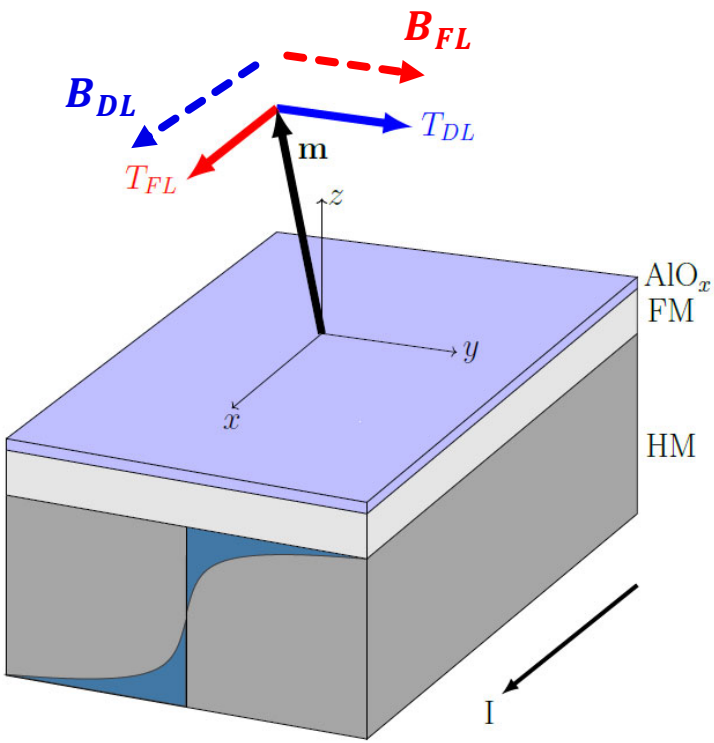
$$\boldsymbol{B}_R = \frac{\alpha_R}{2\mu_B^2}(\boldsymbol{j}_c \times \hat{\boldsymbol{z}})$$

$$\delta m_y = \frac{\mu_B m_e^* \alpha_R}{e\hbar E_F} j_c$$

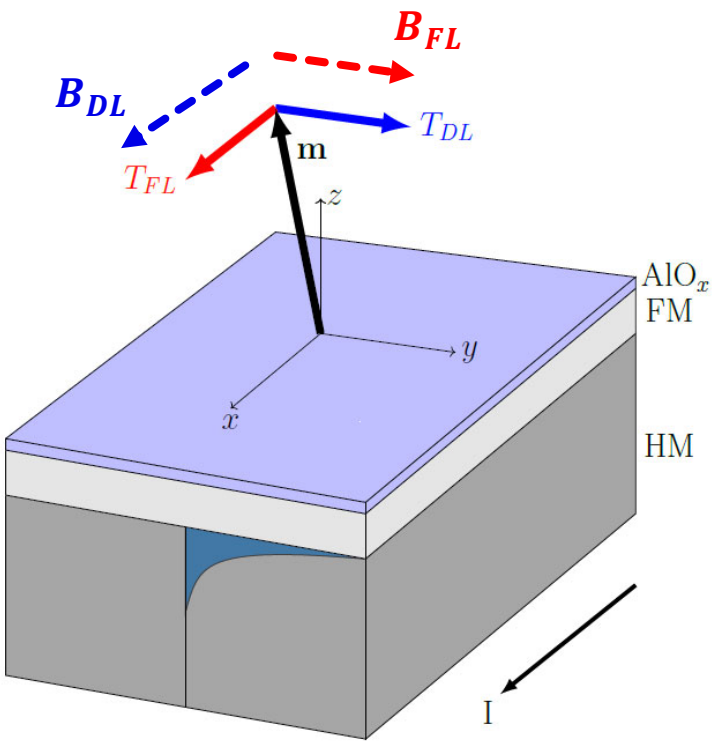
The Rashba field induces a homogenous in-plane spin polarization

Edelstein, Solid State Commun. 1990; Manchon Nat. Mater. 2015; PG and Miron, Phil. Trans. R. Soc. 2011

Current induced spin-orbit torques in FM/NM bilayers



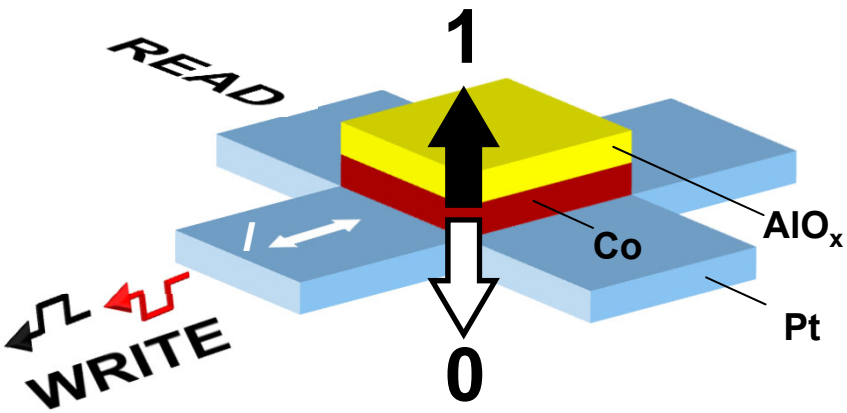
Spin Hall effect

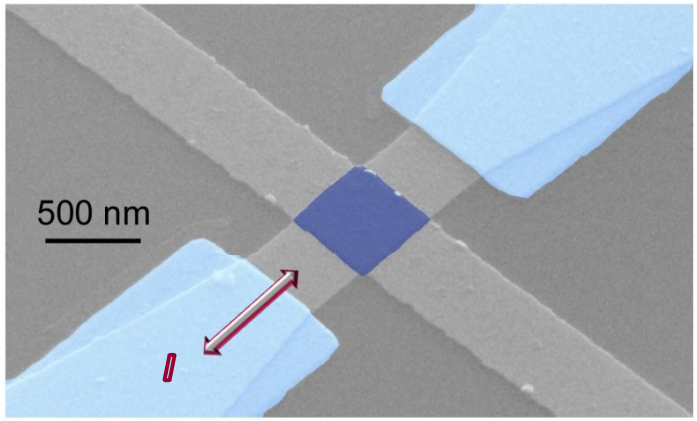


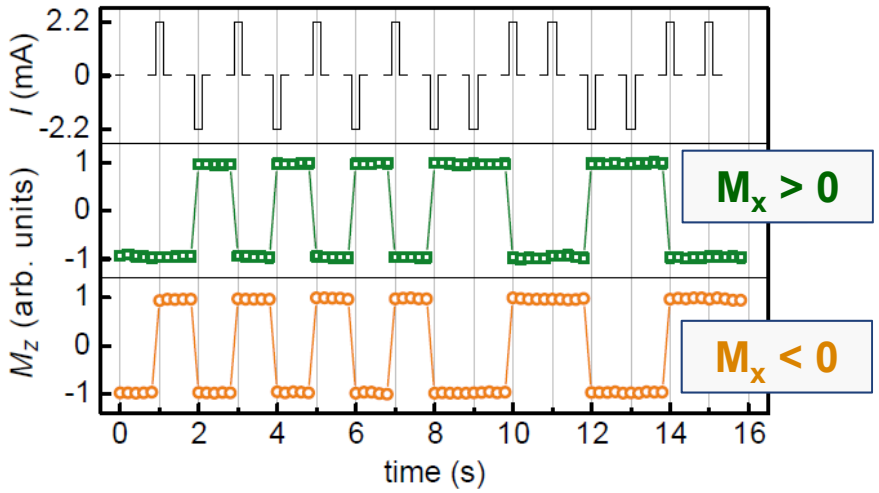
Rashba-Edelstein effect
Interface spin Hall effect
Spin-dependent scattering

Manchon et al., Rev. Mod. Phys. **91**, 035004 (2019)

Spin-orbit torque induced switching of a single ferromagnetic layer



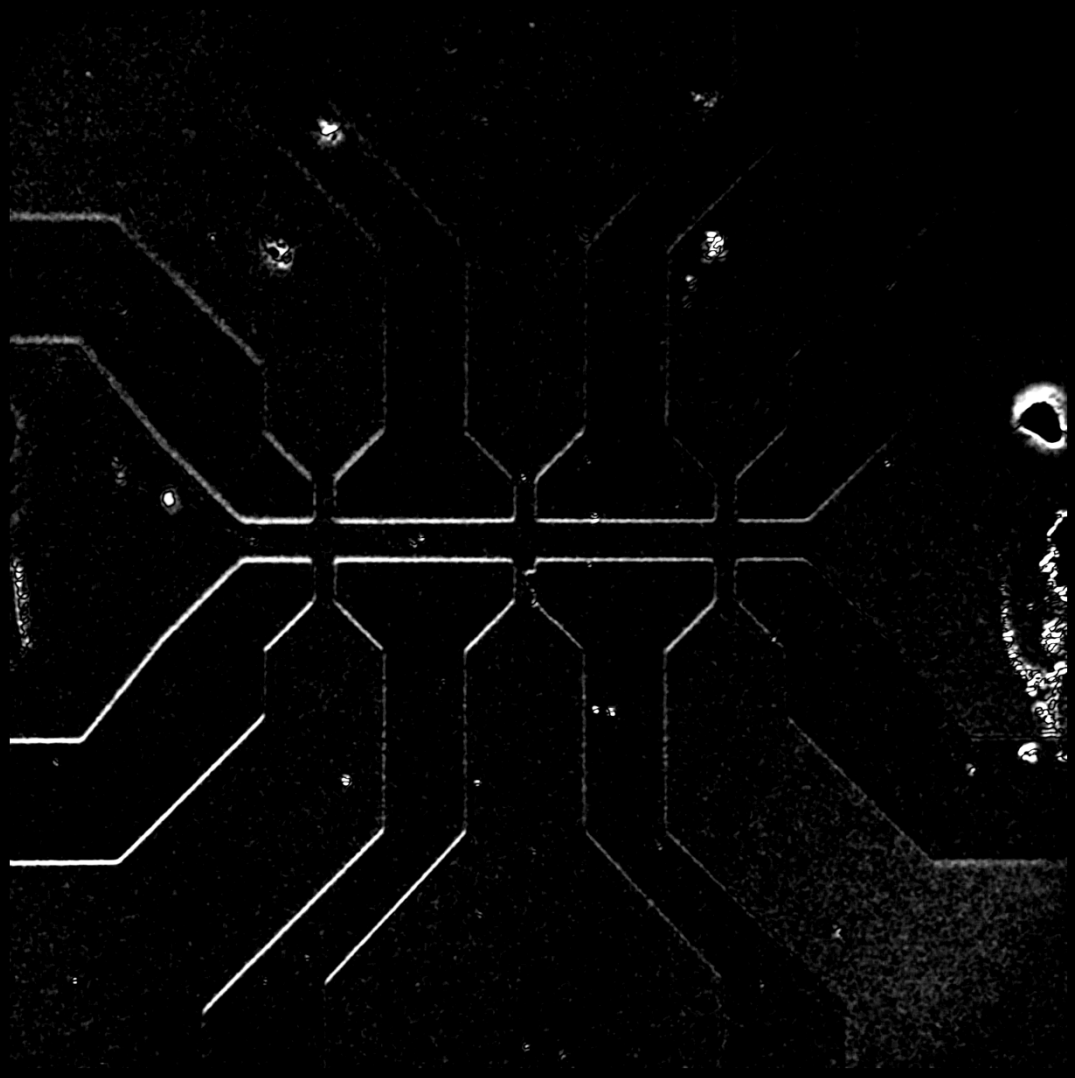




- Transfer of *orbital* to *spin* momentum
- Efficient spin injection/No polarizer
- Compatible with PMA
- Scalable
- CMOS compatible
- Three-terminal devices

Miron et al., *Nature* **476**, 189 (2011)

Current-induced domain wall motion in Pt/TmIG: expansion



p-MOKE

J_x = 10^8 A cm^{-2}

t_p = 250 ns

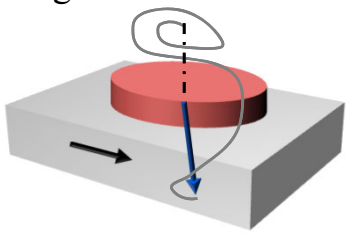
H_x = 215 Oe

Vélez et al., Nat. Comm. **10**, 4750 (2019)

Spin-orbitronics

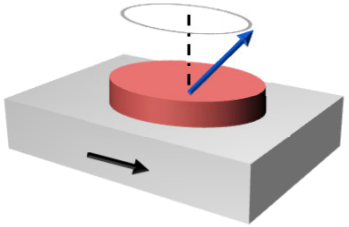
Functionalities & applications

Magnetization switching



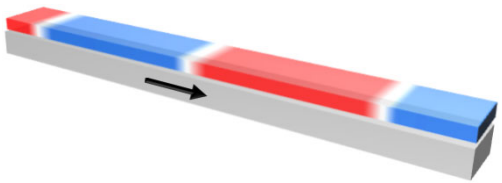
Magnetic memories

High-frequency oscillations



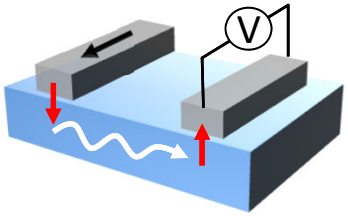
GHz and THz nanooscillators

Domain wall and skyrmion motion



Race-track memories

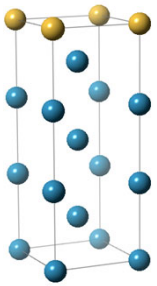
Spin-wave excitations



Chargeless interconnect & spin logic

Materials

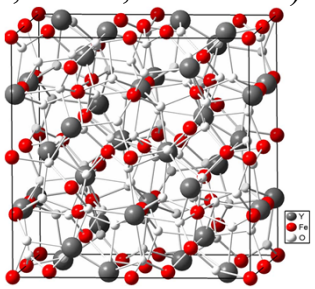
Magnetic metallic heterostructures



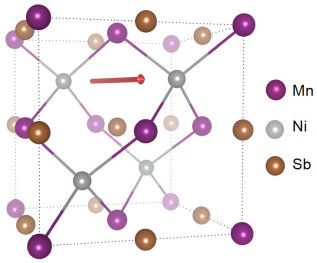
- Co, Ni, Fe, GdFeCo...
- Pt, W, Ta…

WO_x, CuO_x, $SrIrO_3$...
Bi_2Se_3, WTe_2, MoS_2...

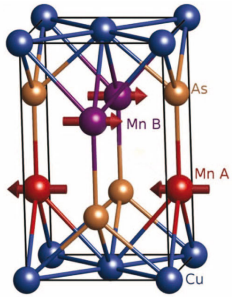
Magnetic Insulators (YIG, TmIG, Bi:YIG…)



Non-centrosymmetric magnets (Ga,Mn)As, MnNiSb…

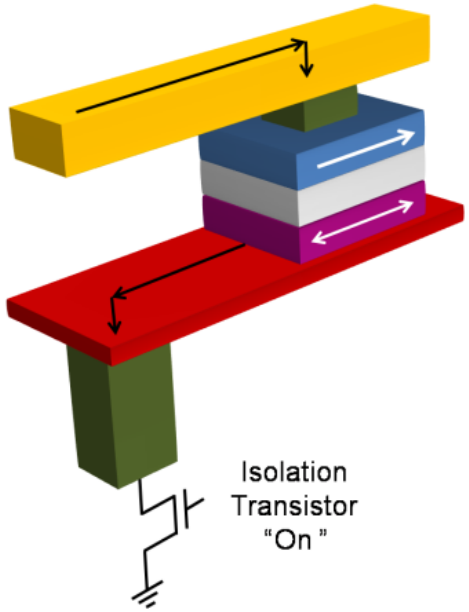


Antiferromagnets (CuMnAs, NiO, IrMn…)

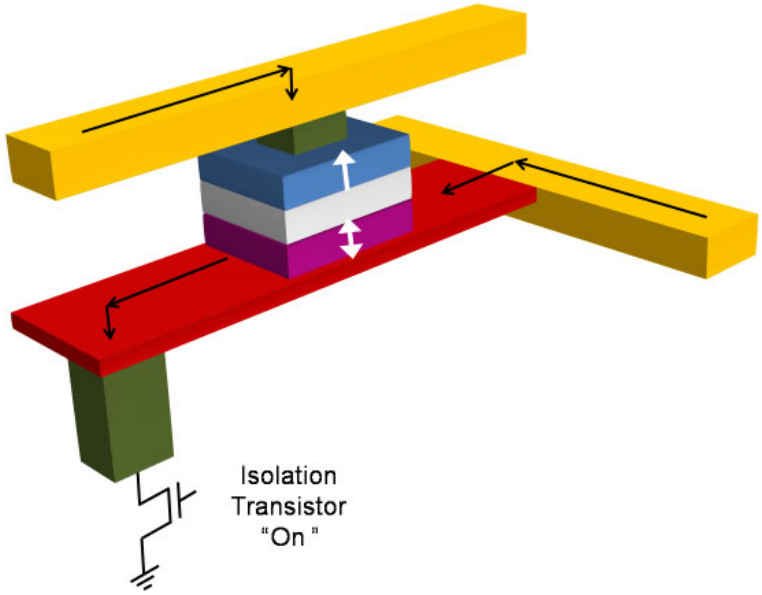


Manchon, PG et al., Rev. Mod. Phys. **91**, 035004 (2019)

Two-terminal vs three-terminal MTJs

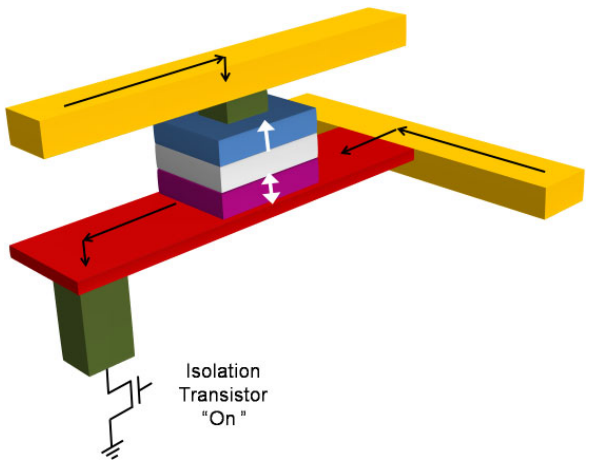


STT-MTJ



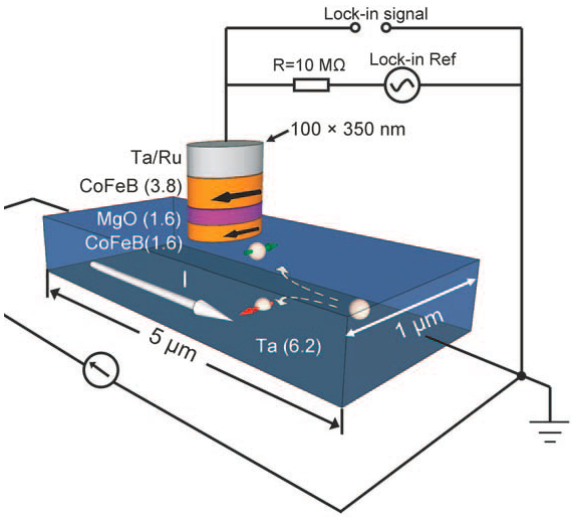
Perpendicular SOT-MTJ

Three-terminal spin-orbit torque MTJs



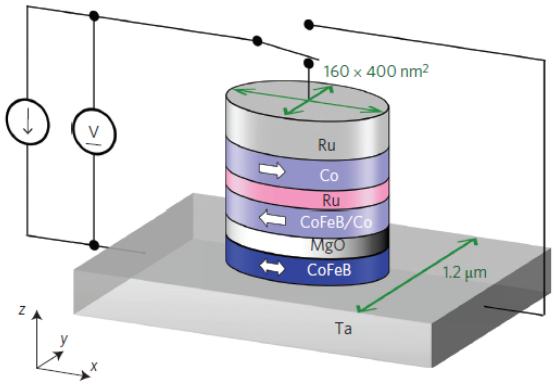
Perpendicular MTJ

Cubukcu et al.,
APL **104**, 042406 (2014)



In-plane MTJ
"y-Type"

Liu et al.,
Science **336**, 555 (2012)

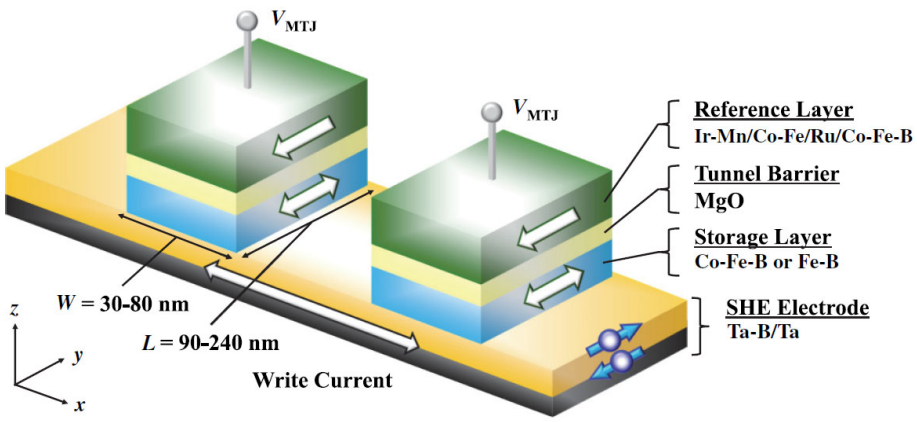


In-plane MTJ
"x-Type"

Fukami et al.,
Nat. Nano. **11**, 621 (2016)

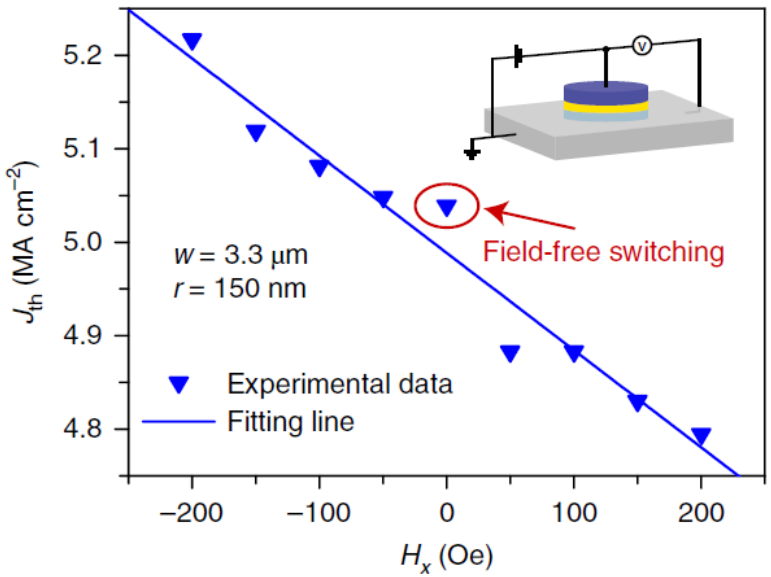
Three terminals are more than two

Voltage-assisted SOT switching of MTJs on a self-aligned Ta-B SOT electrode



Kato et al., Phys. Rev. Appl. **10**, 044011 (2018)

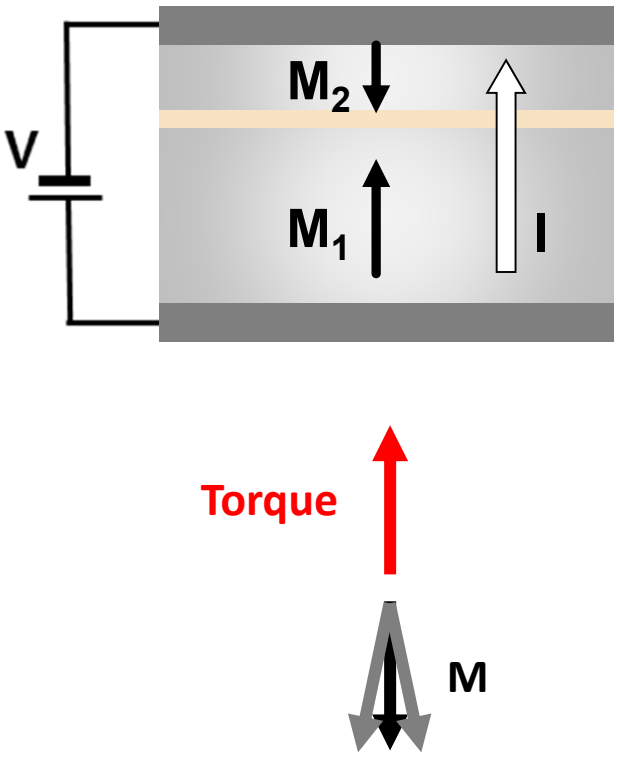
STT + SOT switching at zero field



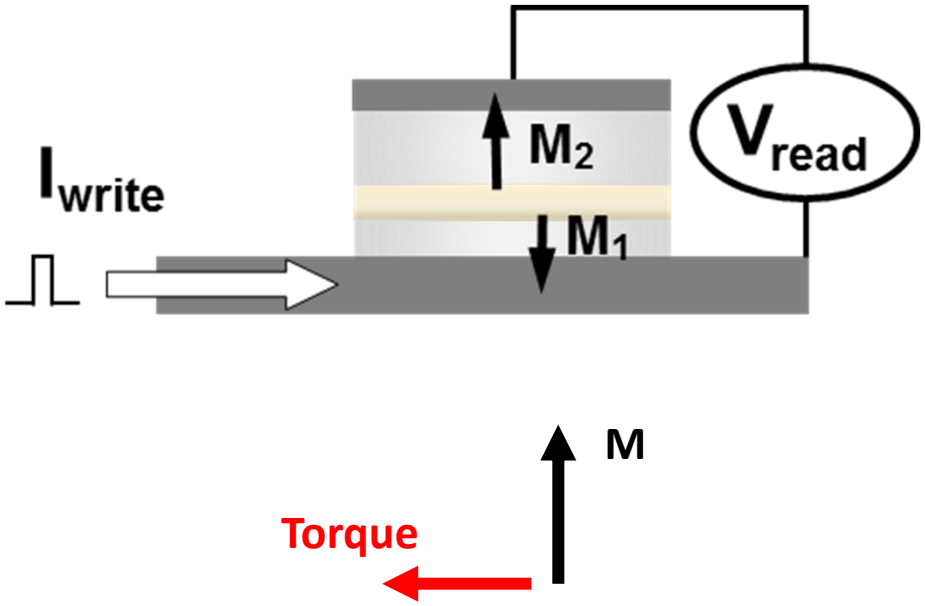
Wang et al., Nat. Electron. **1**, 582 (2018)

STT vs SOT magnetization dynamics

STT - MTJ

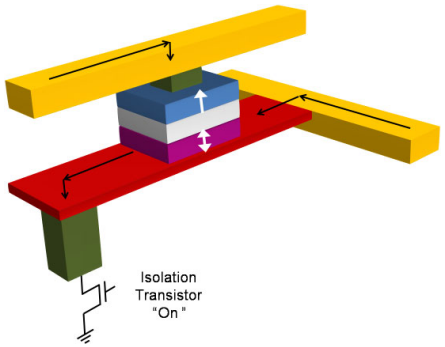


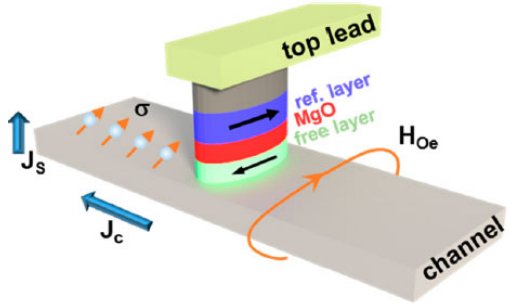
SOT - MTJ

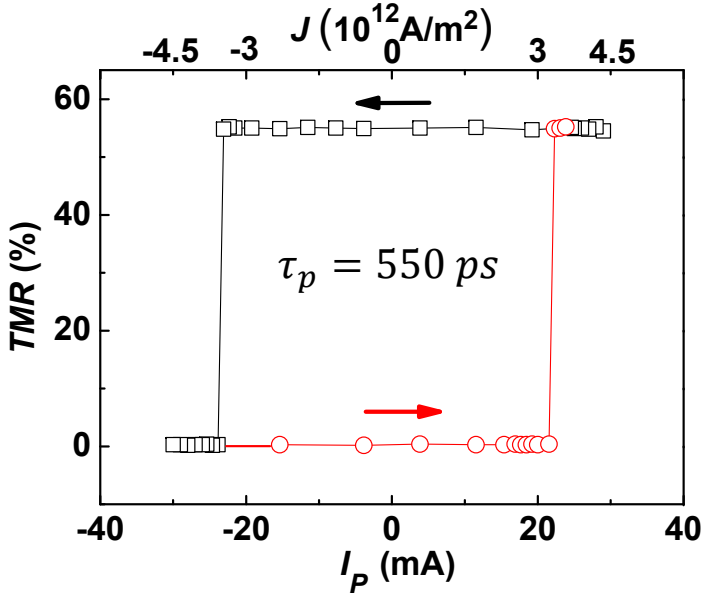


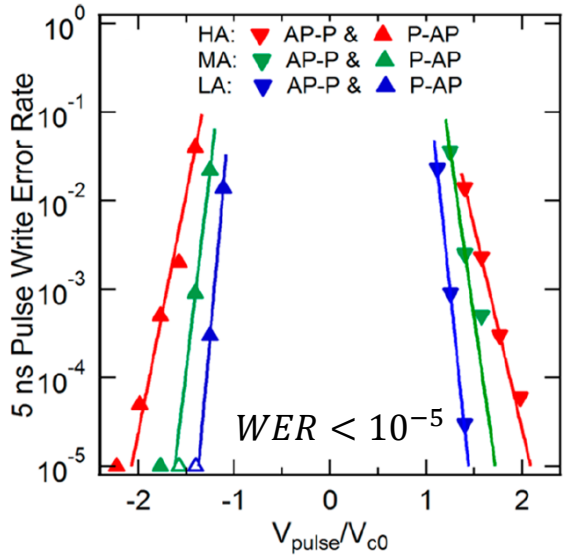
- Delayed
- Instantaneous

Fast and reliable switching of SOT-MTJs









Cubukcu et al., IEEE TM **54**, 9300204 (2018)

Cubukcu et al., APL **104**, 042406 (2014)

Aradhya et al., Nano Lett. **16**, 5987 (2016)

Time-resolved measurements of 3-terminal MTJs driven by SOT, STT, VCMA

Imec - Interuniversity Microelectronics Centre, Leuwen, Belgium

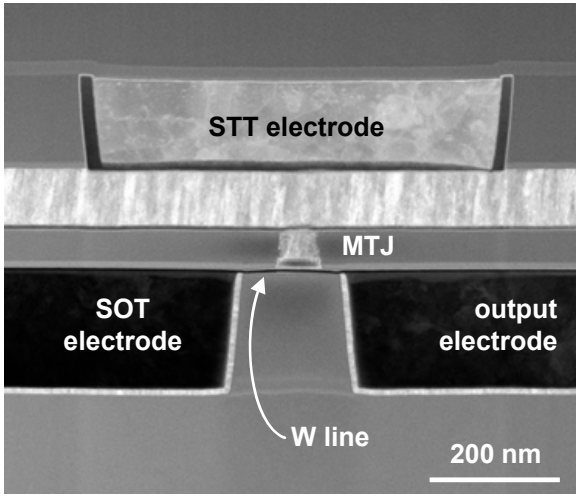
K. Garello, F. Yasin, S. Couet, G.S. Kar

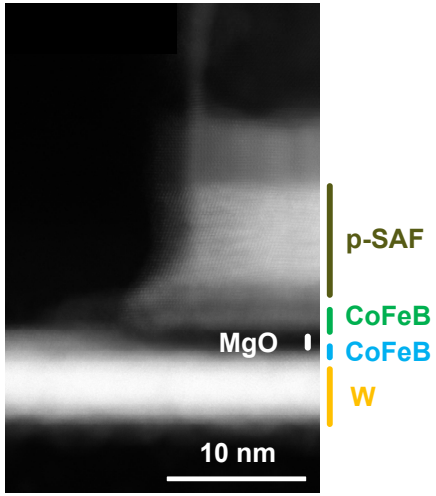
ETH Zurich

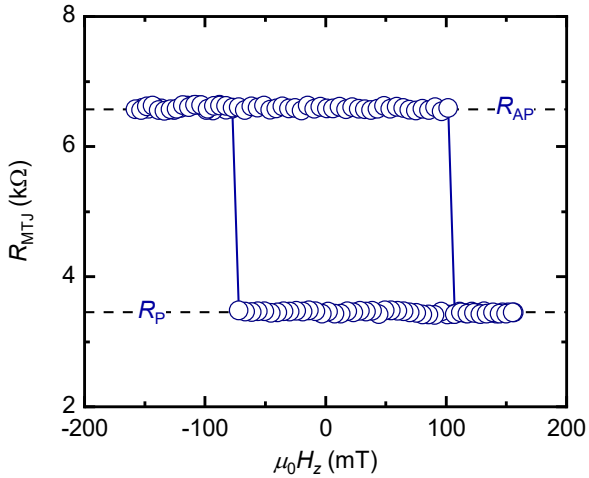
E. Grimaldi, V. Krizakova, G. Sala, PG

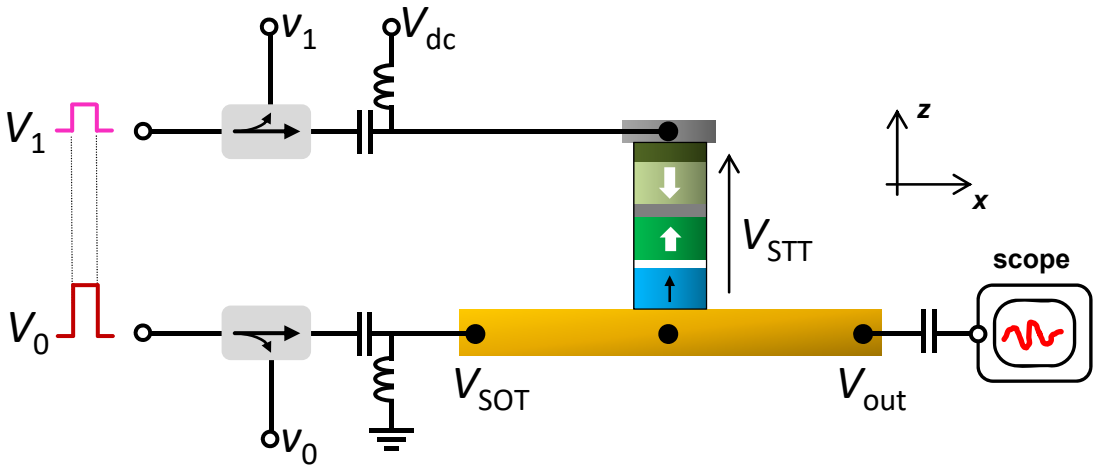
imec

Three-terminal SOT-MTJ





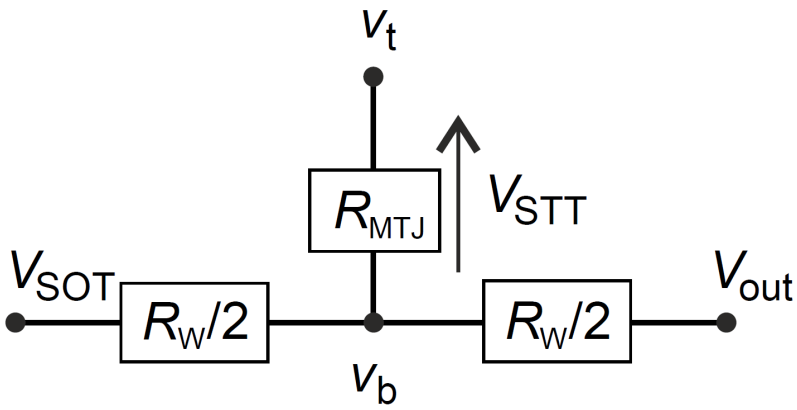




Samples fabricated at imec

E. Grimaldi, V. Krizakova, K. Garello, PG et al., Nat. Nanotech. **15**, 111 (2020)

Bias voltages in a three-terminal SOT-MTJ



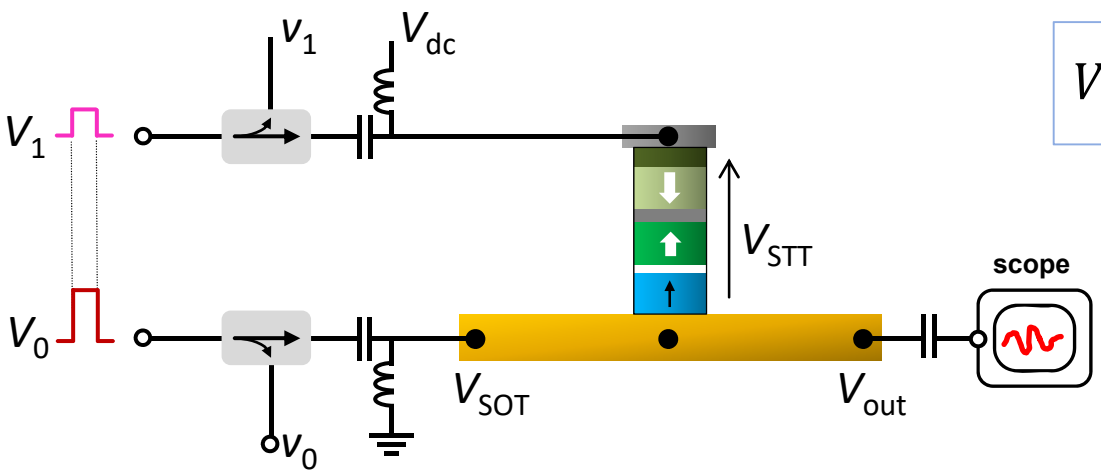
$$V_{STT} = \left(v_t - \frac{V_{SOT}}{2}\right) \Big/ \left(1 + \frac{R_W}{4R_{MTJ}}\right)$$

Assuming $R_W \ll R_{MTJ}$

$$V_{STT} \approx v_t - 0.5\, V_{SOT}$$

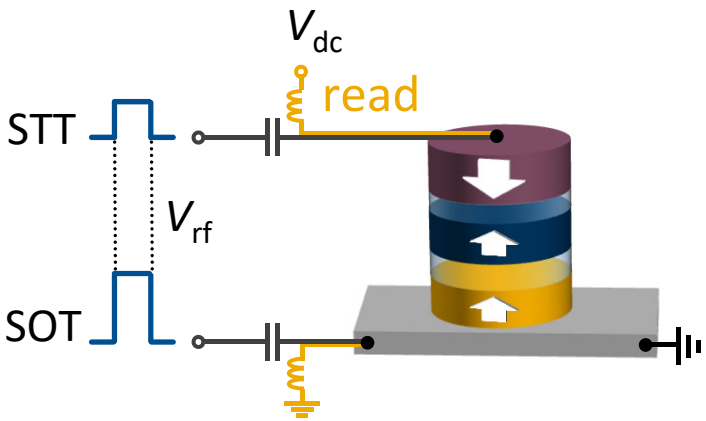
$$\downarrow$$

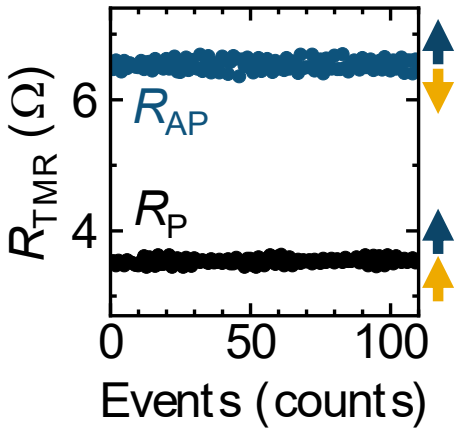
$$\boxed{V_{STT} \approx 1.09 \left(\frac{V_0}{V_1} - 0.46\right) V_{SOT}}$$

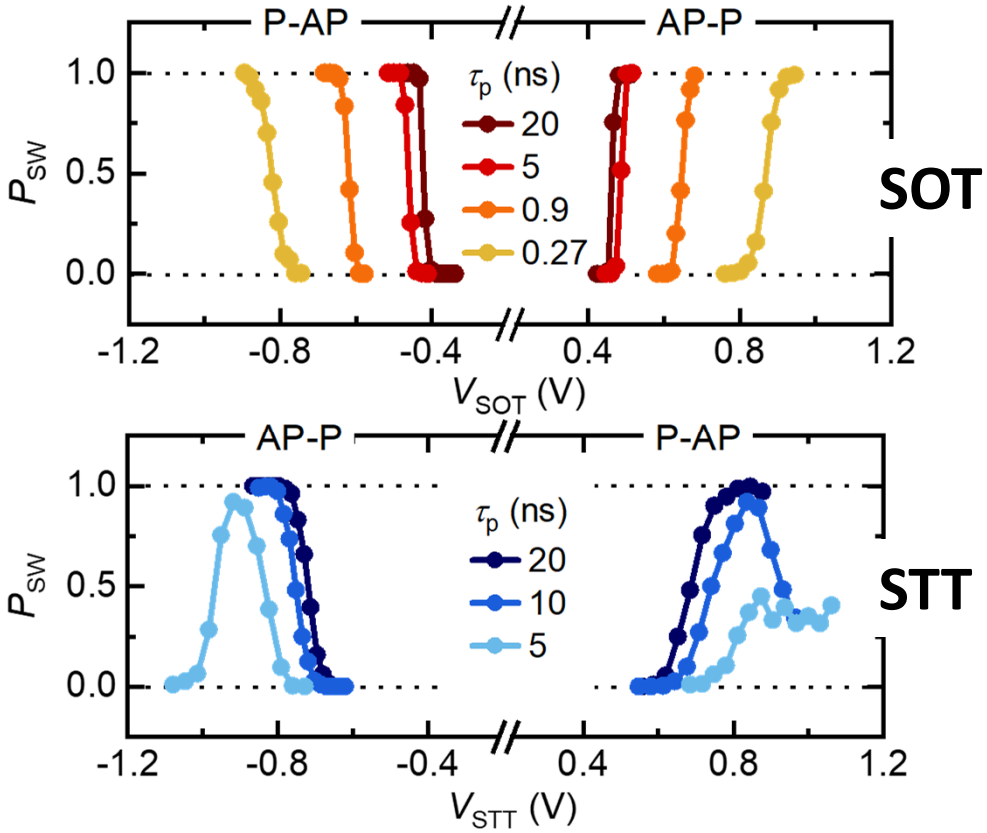


E. Grimaldi, V. Krizakova, K. Garello, PG et al., Nat. Nanotech. **15**, 111 (2020)

After-pulse switching probability





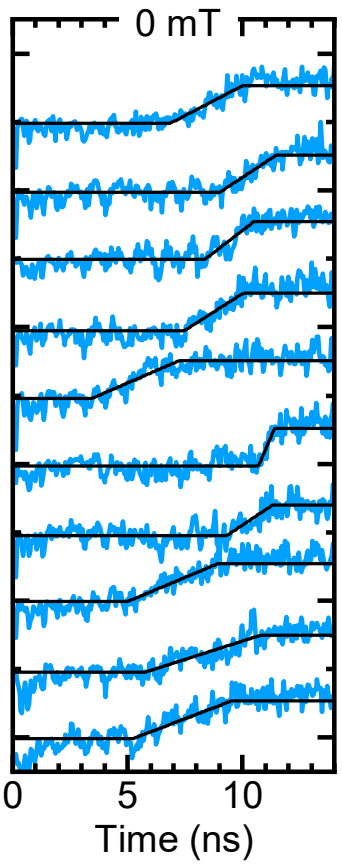


E. Grimaldi, V. Krizakova, K. Garello, PG et al., Nat. Nanotech. **15**, 111 (2020)

Single-shot measurements of SOT switching in a 3T-MTJ

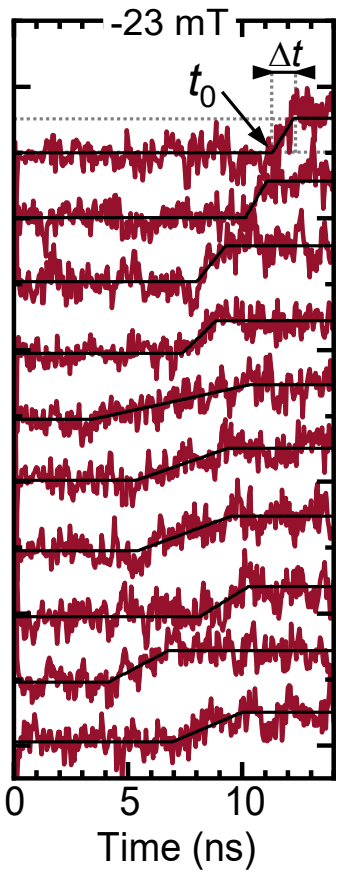
STT only

$V_{SOT} = 0$
$V_{STT} = +0.88\ V$



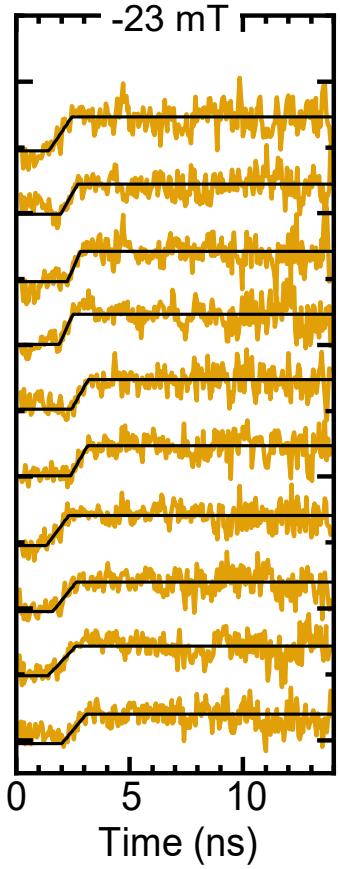
SOT - STT

$V_{SOT} = 0.45\ V$
$V_{STT} = -0.23\ V$



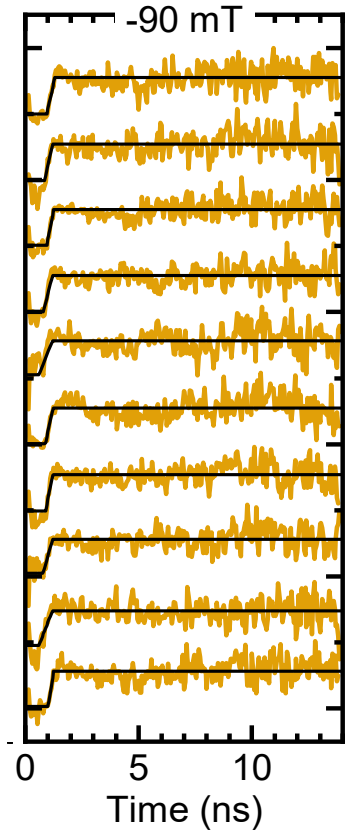
SOT + STT (VCMA)

$V_{SOT} = 0.45\ V$
$V_{STT} = +0.27\ V$



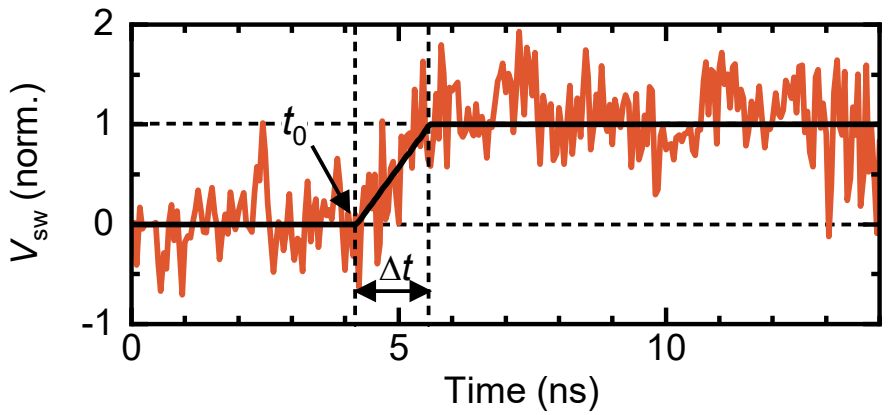
SOT + STT (VCMA) + field

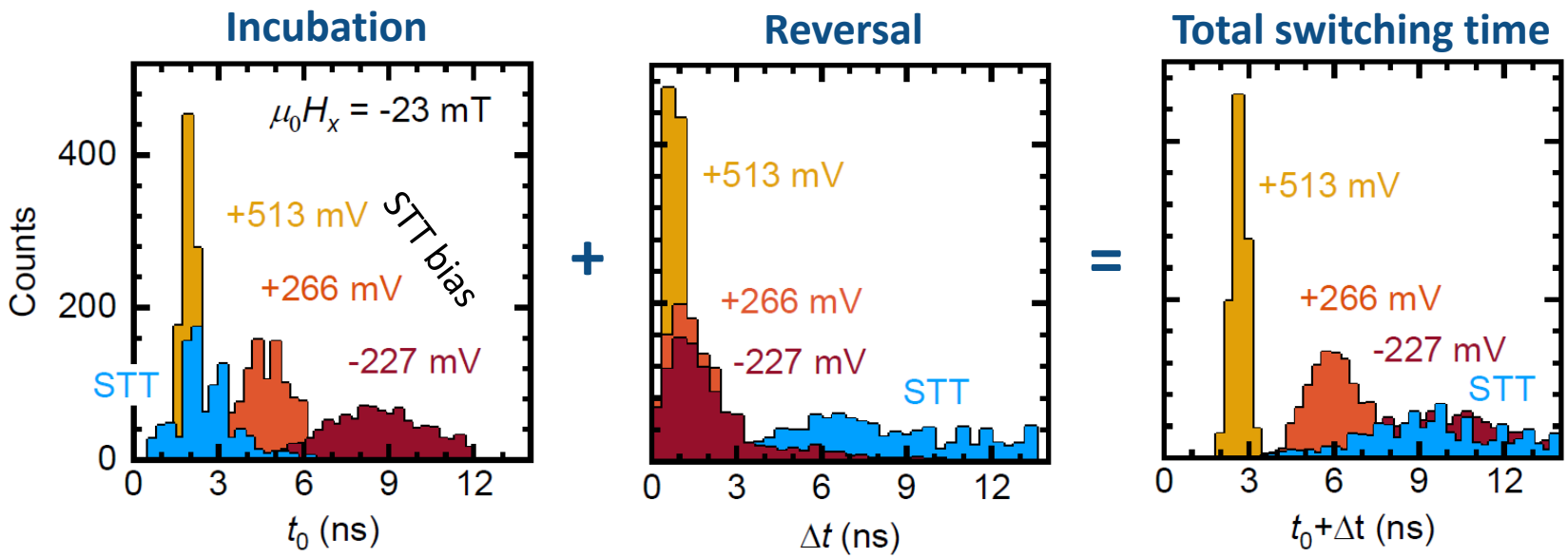
$V_{SOT} = 0.45\ V$
$V_{STT} = +0.51\ V$



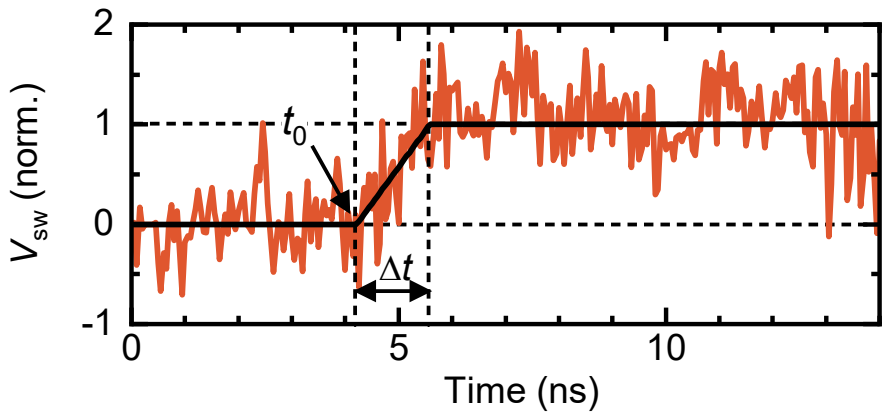
E. Grimaldi, V. Krizakova, K. Garello, PG et al., Nat. Nanotech. **15**, 111 (2020)

Analysis of single-shot SOT switching events at low in-plane field

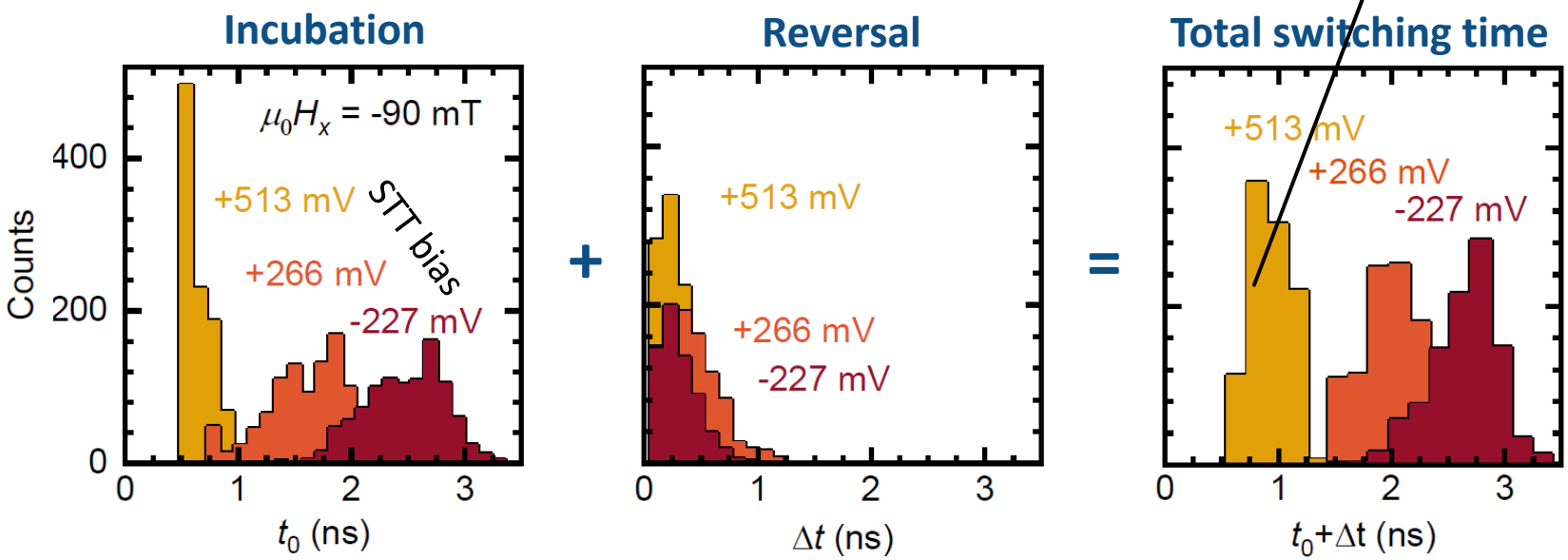




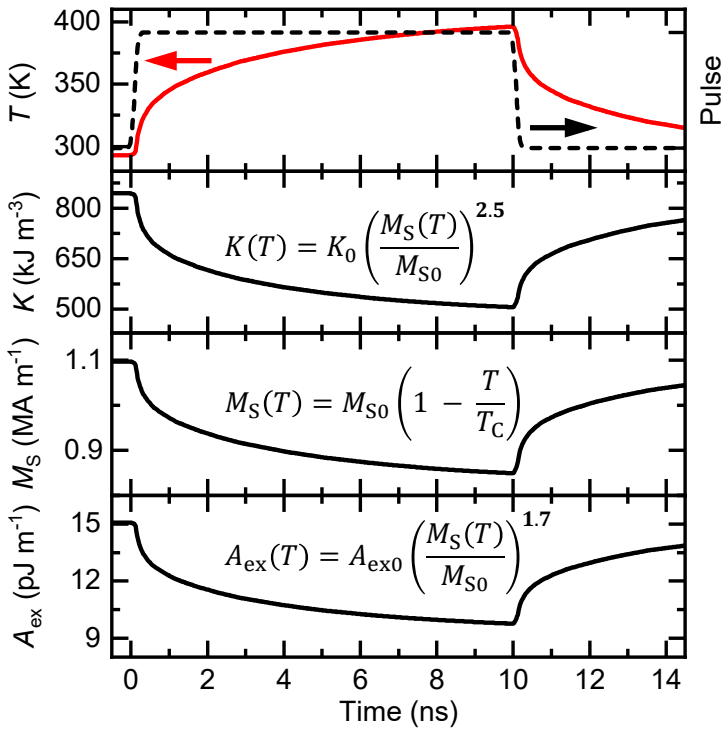
Analysis of single-shot SOT switching events at large in-plane field

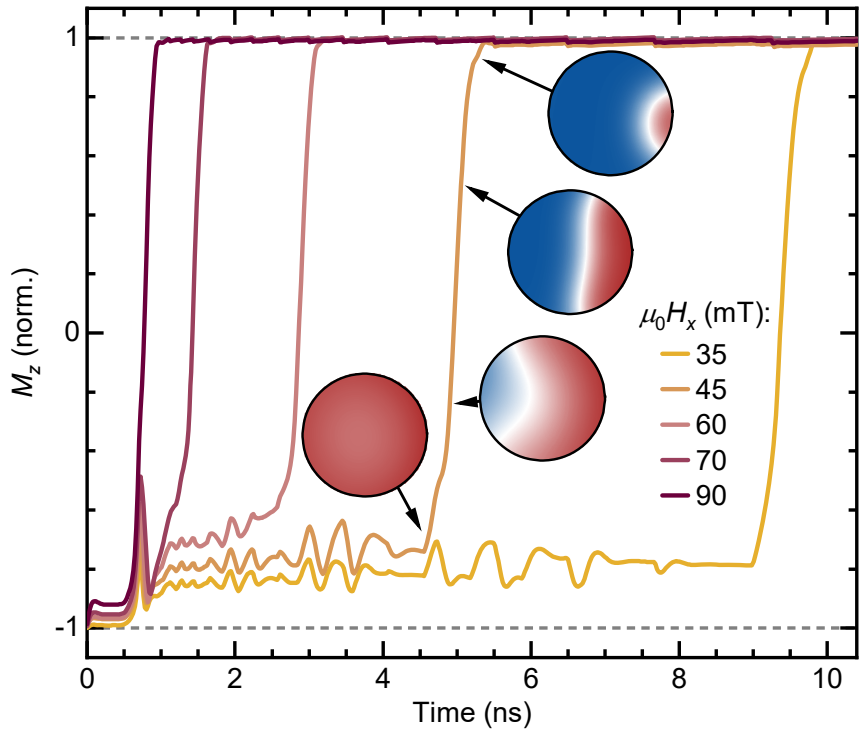


$t_0 + \Delta t = 0.9 \pm 0.16\ ns$



Origin of the incubation and reversal time in SOT switching

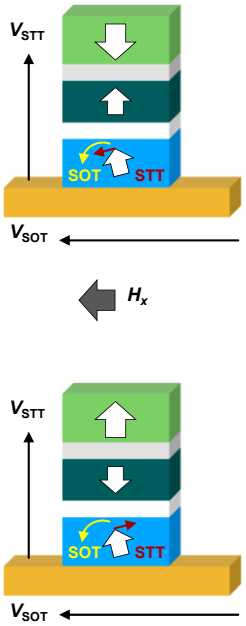




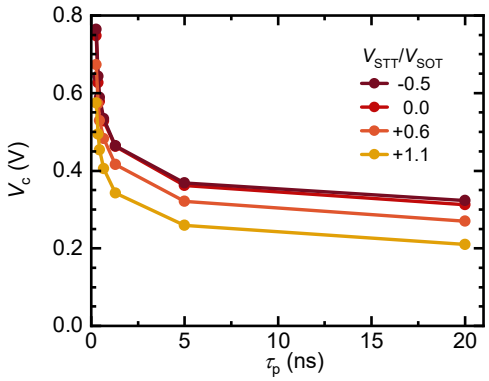
E. Grimaldi, V. Krizakova, K. Garello, PG et al., Nat. Nanotech. **15**, 111 (2020)

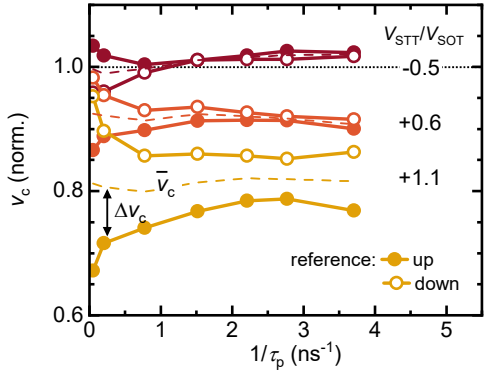
Baumgartner et al., Nat. Nanotech. **12**, 980 (2017)

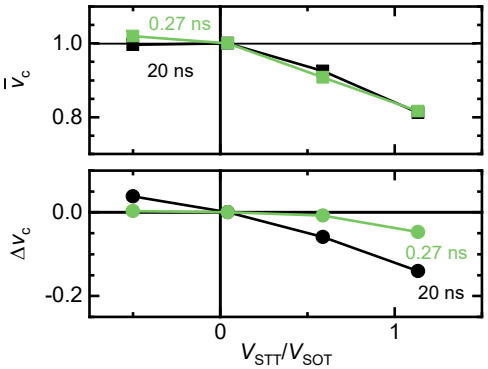
Separating the effects of STT and VCMA (voltage control of magnetic anistropy)



Critical SOT switching voltage vs $\frac{V_{STT}}{V_{SOT}}$ ratio







VCMA:

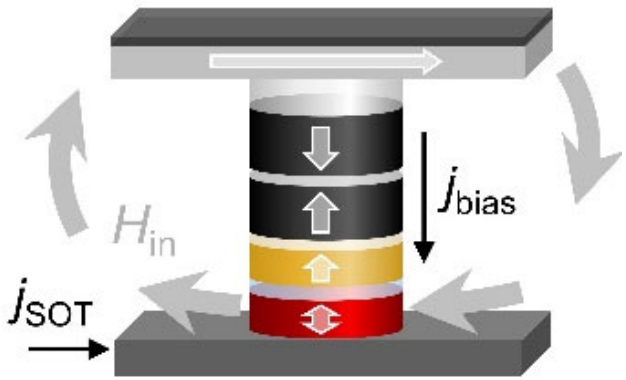
$$\bar{v}_c = (v_c^{\uparrow} + v_c^{\downarrow})/2$$

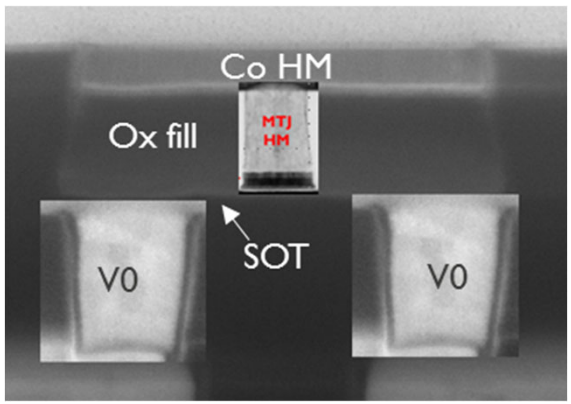
STT:

$$\Delta v_c = (v_c^{\uparrow} - v_c^{\downarrow})/2$$

E. Grimaldi, V. Krizakova, K. Garello, PG et al., Nat. Nanotech. **15**, 111 (2020)

Field-free SOT switching of a 3-terminal MTJ below 1 ns

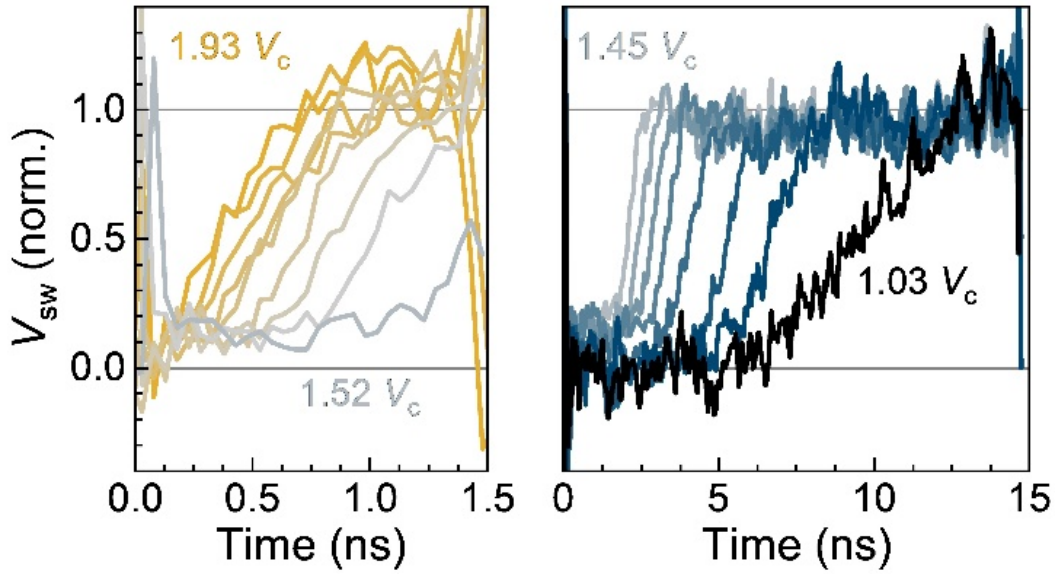




imec

Garello et al.,
IEEE Symp. VLSI Technol., T194 (2019)

$$H_{ext} = 0$$



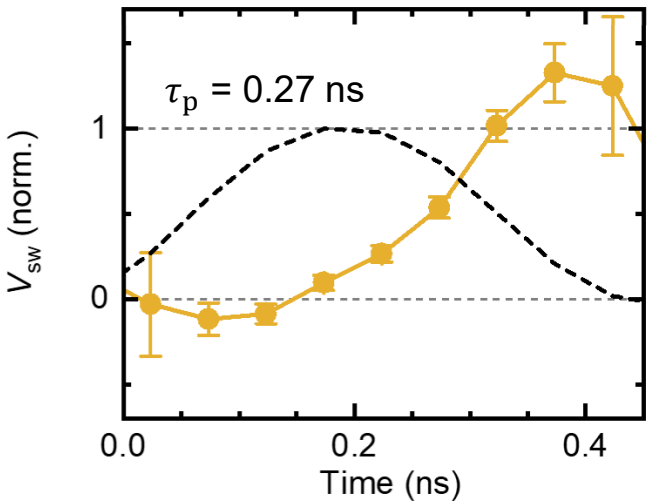
V. Krizakova, K. Garello, PG et al.,
Appl. Phys. Lett. **116**, 232406 (2020)

SOT vs STT switching: speed and efficiency

STT is more efficient than STT at large $\tau_p \geq 5\ ns$

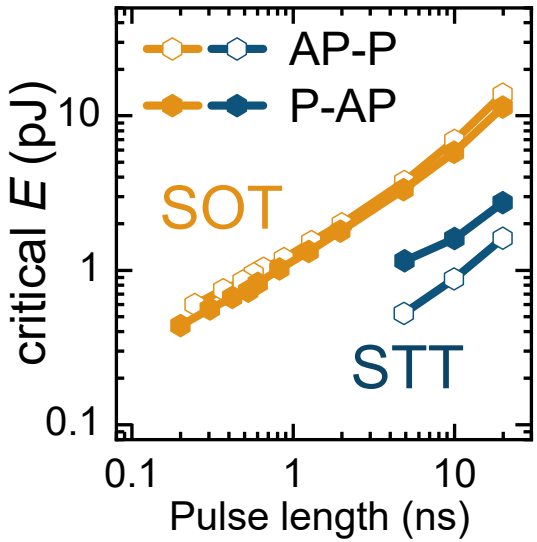
SOT reaches maximum efficiency at $\tau_p < 1\ ns$

SOT-only:
≈ 100 % switching probability
@ 0.3 ns



V_{SOT} = +997 mV
V_{STT}/V_{SOT} = −0.5
$\mu_0 H_x$ = +23 mT

$E_c(\tau_p) = V_c^2 \tau_p / R$



$V_{c,SOT}$ = 0.4 V
$j_{c,SOT}$ = 2.0 × 10^8 A cm^{-2}

$V_{c,STT}$ = 0.75 V
$j_{c,STT}$ = 4.2 × 10^6 A cm^{-2}

E. Grimaldi, V. Krizakova, K. Garello, PG et al., Nat. Nanotech. **15**, 111 (2020)

SOT-MRAMs: figures of merit

Cell size (cost): > STT, < SRAM

Write energy: > STT

Write speed: > STT

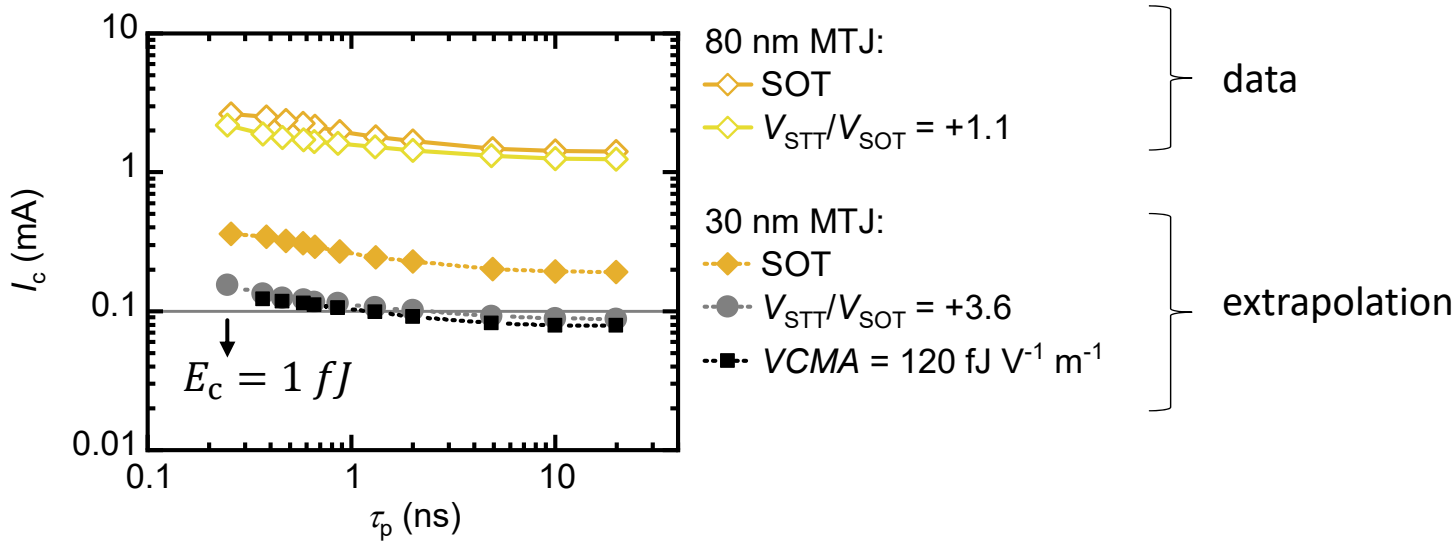
Read speed: > STT at equal RDR

Endurance: > STT at high speed

CMOS compatibility: ok

→

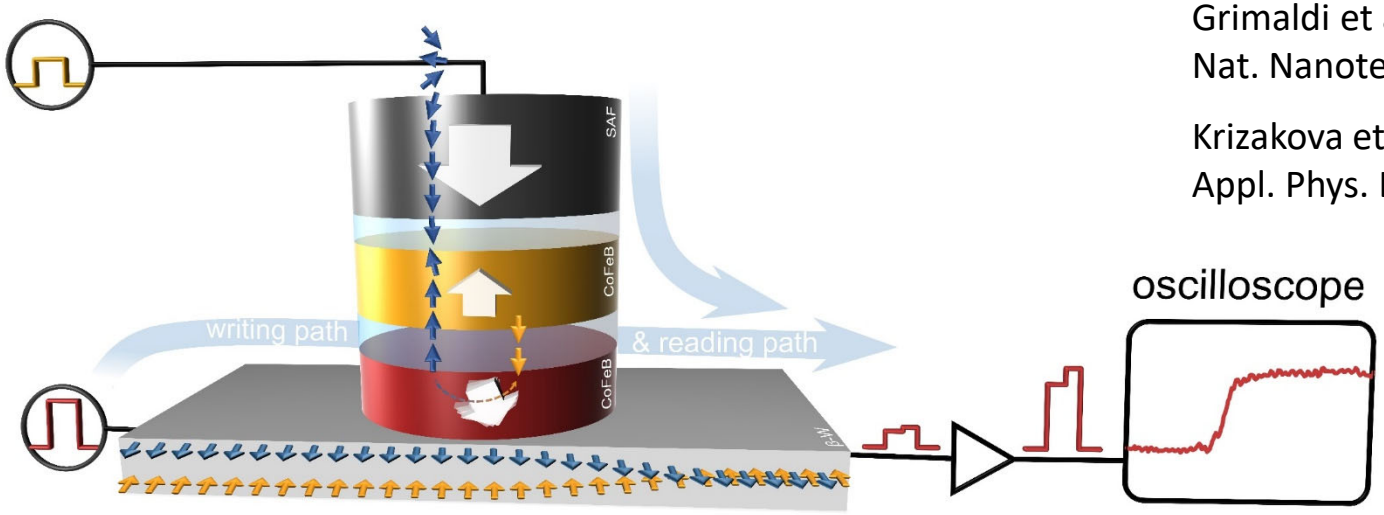
- *Downscale* the MTJ and SOT current line
- Increase the *STT bias*.
- Exploit the *VCMA effect*.
- Increase the *SOT efficiency*



E. Grimaldi, V. Krizakova, K. Garello, PG et al., Nat. Nanotech. **15**, 111 (2020)

Conclusions #1

- Single-shot dynamics driven by SOT in 3-terminal MTJs
- SOT incubation time due to strong anisotropy preventing domain nucleation
- Interplay of SOT, STT, VCMA, and Joule heating
- Extremely narrow switching time distributions can be achieved (std < 0.16 ns)
- ≈ 100% SOT switching rate at 0.3 ns at $V_{SOT} \approx 2V_c$
- Sub-ns field-free SOT switching with MTJ hard magnetic mask
- SOT becomes energy-competitive below 1 ns
- Strategies to improve SOT efficiency



Grimaldi et al.,
Nat. Nanotech. **15**, 111 (2020)

Krizakova et al.,
Appl. Phys. Lett. **116**, 232406 (2020)

ETH zürich

Magnetic logic circuits driven by spin-orbit torques

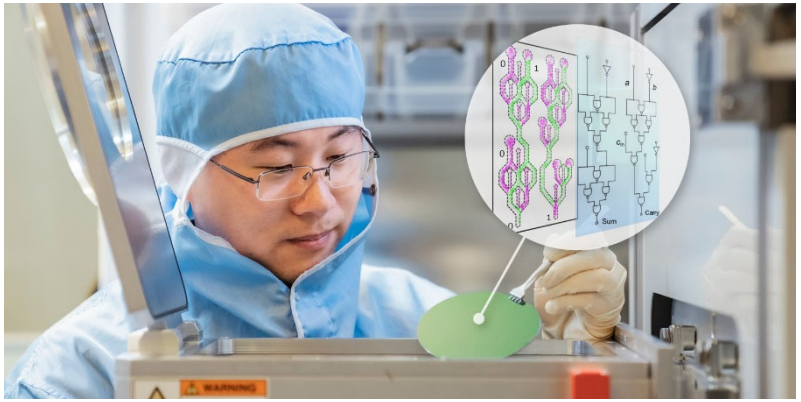
ETH Zürich & Paul Scherrer Institute

***Lab for Mesoscopic system*:**

Zhaochu Luo, Aleš Hrabec, Eugenie Kirk,

Jizhai Cui, Anja Weber, Sina Mayr,

Laura Heyderman



***Lab for Magnetism and Interface Physics*:** Phuong Dao, Manuel Baumgartner,

Gunasheel Krishnaswamy, Giacomo Sala, Junxiao Feng, Pietro Gambardella

Paul Scherrer Institute

***Swiss Light Source*:** Jaianth Vijayakumar, Tatiana Savchenko, Simone Finizio,

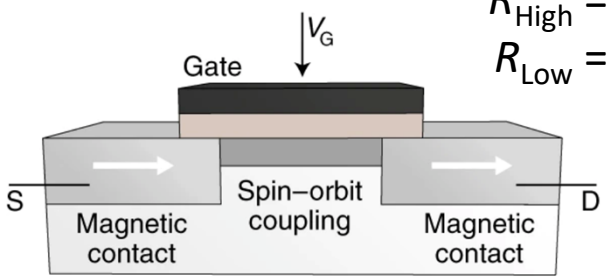
Armin Kleibert, Jörg Raabe

***Lab for Micro &Nanotechnology*:** Vitaliy Guzenko

Proposals for spin-based logic devices

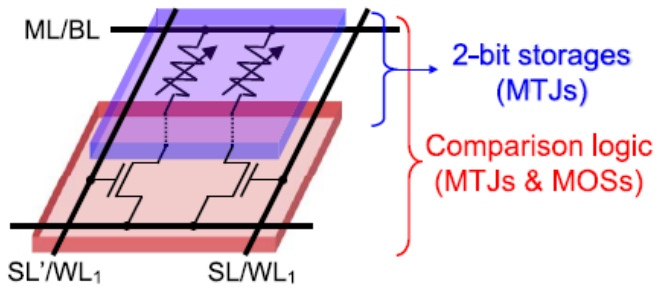
Spin transistor

R_{High} = '0'
R_{Low} = '1'



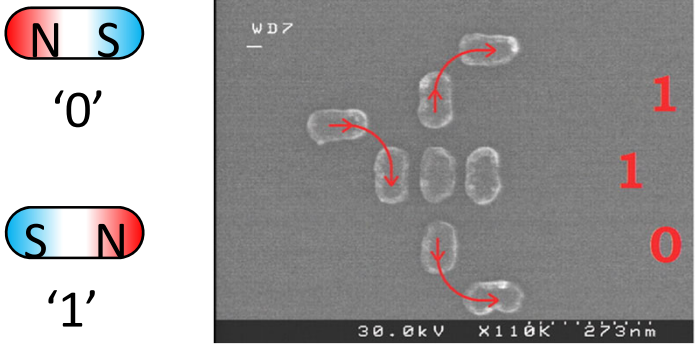
S.Datta et al. ***APL*** (1990)

MRAM-based logic-in-memory



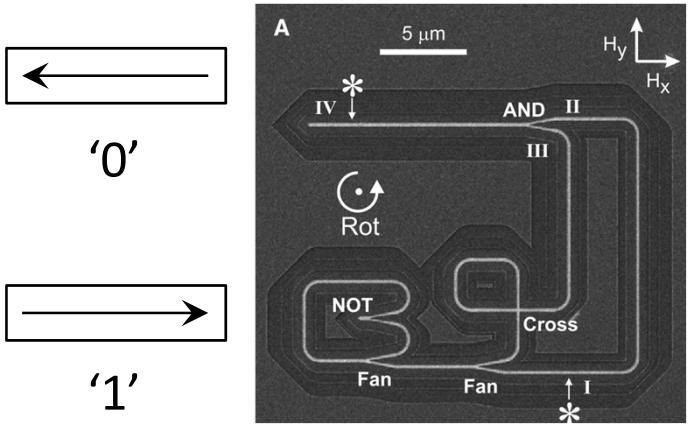
T. Hanyu et al. ***Proc. IEEE*** (2016)

Nanomagnet logic



A.Imre et al. ***Nature*** (2006)

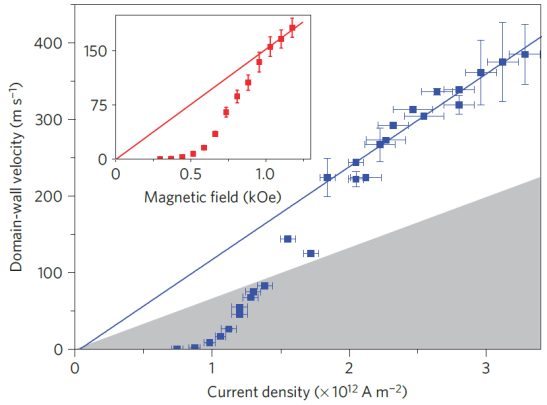
Magnetic domain-wall logic



D.Allwood et al. ***Science*** (2005)

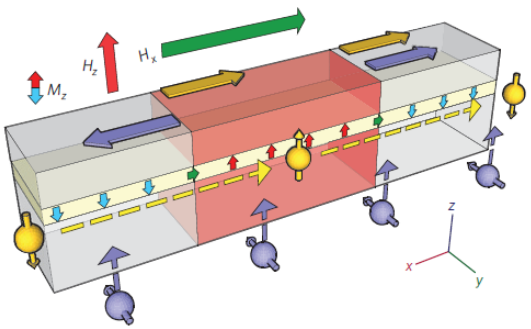
SOT-driven magnetic domain walls

High speed



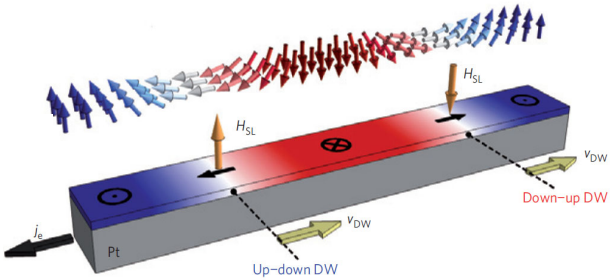
Miron et al., *Nat. Mater*. 2011
Cai et al., *Nat. Electr*. 2020

Depinning



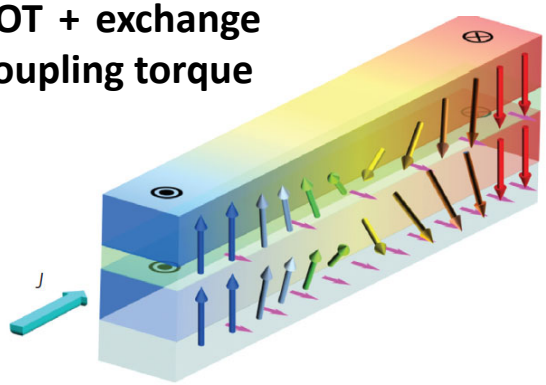
Haazen et al., *Nat. Mater*. 2013

Interplay of DMI and SOT



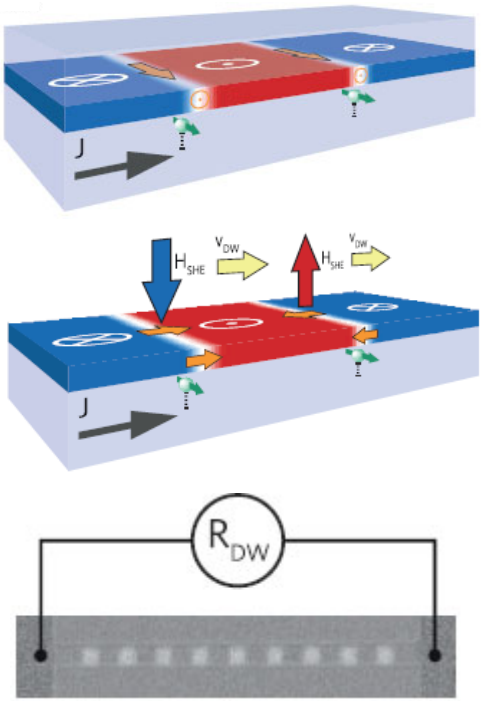
Thiaville et al., *Europhys. Lett*. 2012
Emori et al., *Nat. Mater*. 2013

SOT + exchange coupling torque



Yang, Ryu &Parkin, *Nat. Nano*. 2015

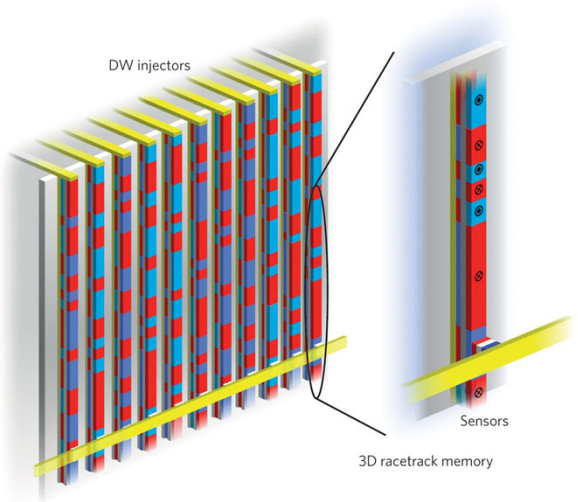
Chirality control and positioning of DW



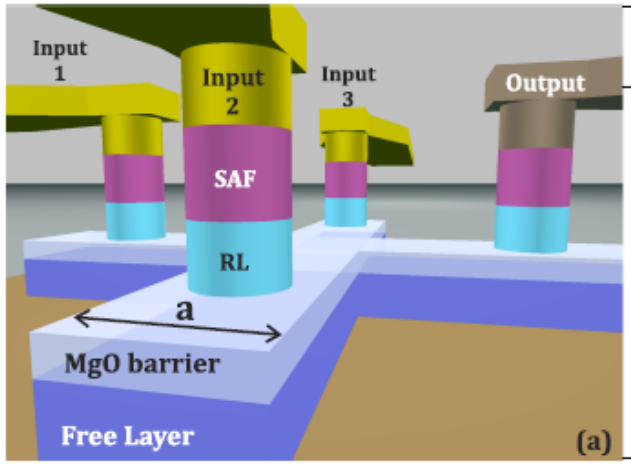
Franken et al., *Sci. Rep*. 2014
Chen et al., *Nat. Comm*. 2013

Advantages of magnetic DW logic

- Complete set of logic elements → arbitrary logic circuit
- Same objects for logic inputs and outputs → easy cascade
- Logic gate defined by geometric structure → flexible design
- Emerging current-driven domain-wall memory devices



Parkin & Yang, *Nature Nano*. 2015



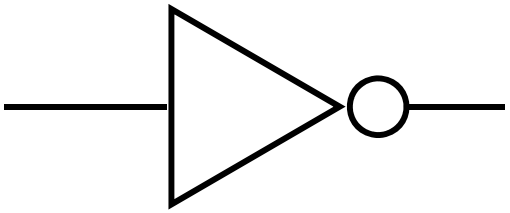
Input 1	Input 2	Input 3	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

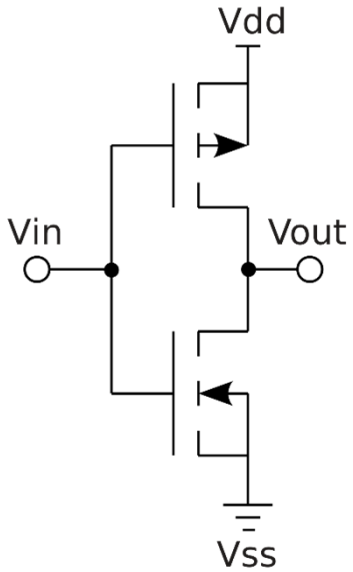
Manfrini et al. *AIP Adv*. (2018)

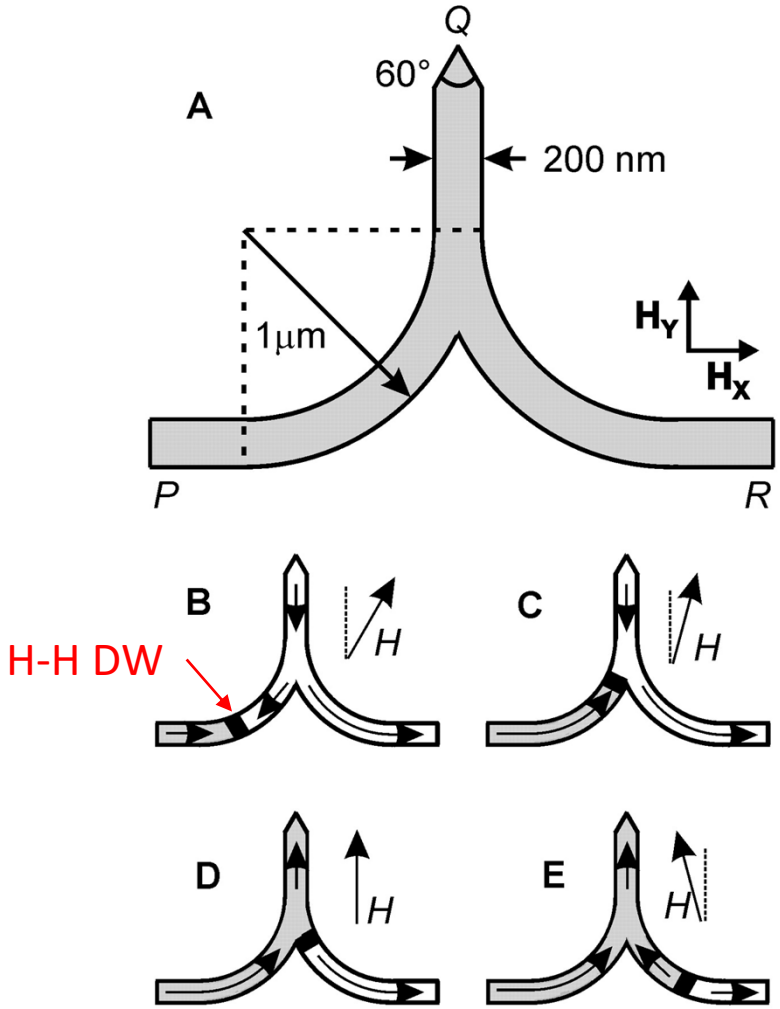
Zhao et al., IEEE Trans. Mag. 2011
Chang et al., IEEE J. Expl. Sol. State Comp. Dev. 2016
…

Implementing basic logic gates is not always straightforward…

NOT gate

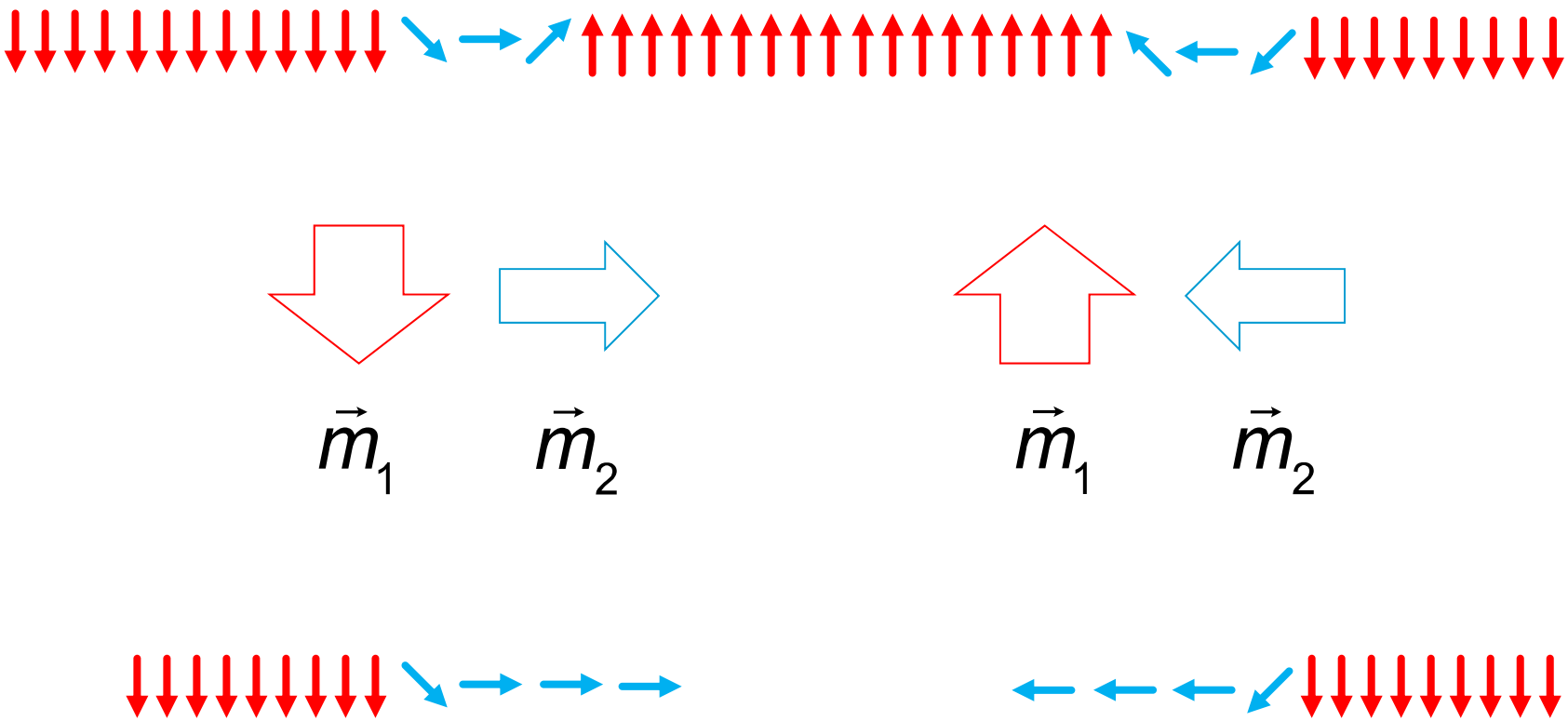






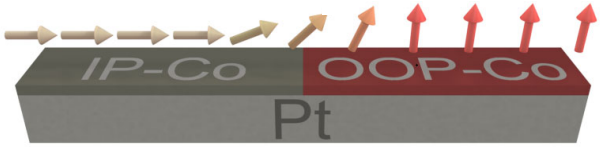
D.Allwood et al. ***Science*** (2002)

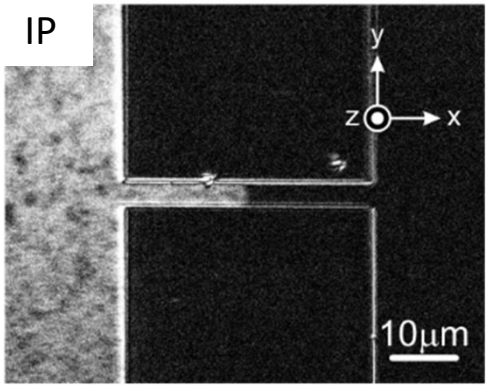
From chiral Néel walls to chirally-coupled nanomagnets

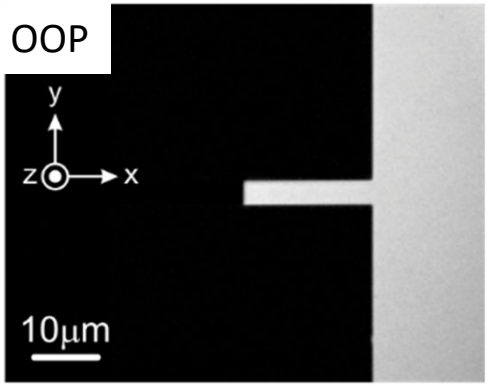


$$H_{\mathrm{DM}} = -\vec{D}_{12} \cdot (\vec{m}_1 \times \vec{m}_2)$$

Control of magnetic anisotropy by selective oxidation of Pt/Co/Al



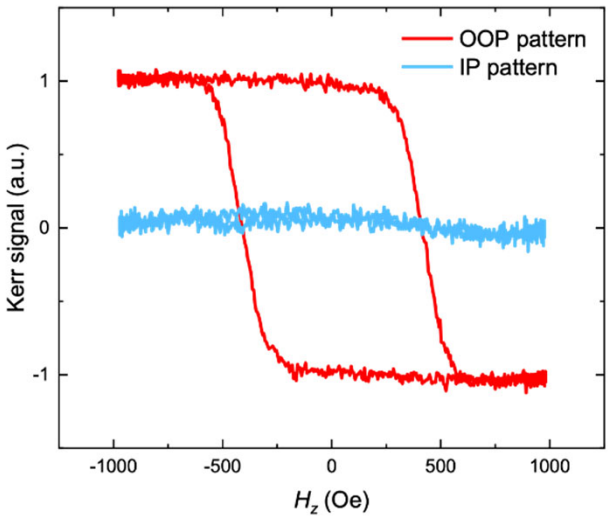


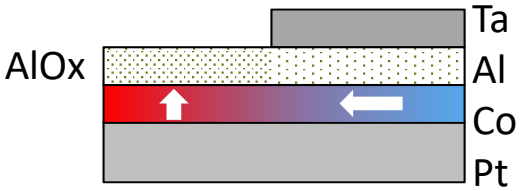


Dao et al., Nano Lett. 19, 5930 (2019)

Pt(6 nm)/Co(1.6 nm)/Al (2 nm)

Pt(6 nm)/Co(1.6 nm)/AlOx (2 nm)





CONTROL OF MAGNETIC ANISOTROPY

Oxidation

Monso et al., Appl. Phys. Lett. 2002

Rodmacq et al., Phys. Rev. B 2009

Ion irradiation

Fassbender et al., J. Phys. D 2004

Haazen, Nat. Mat. 2013

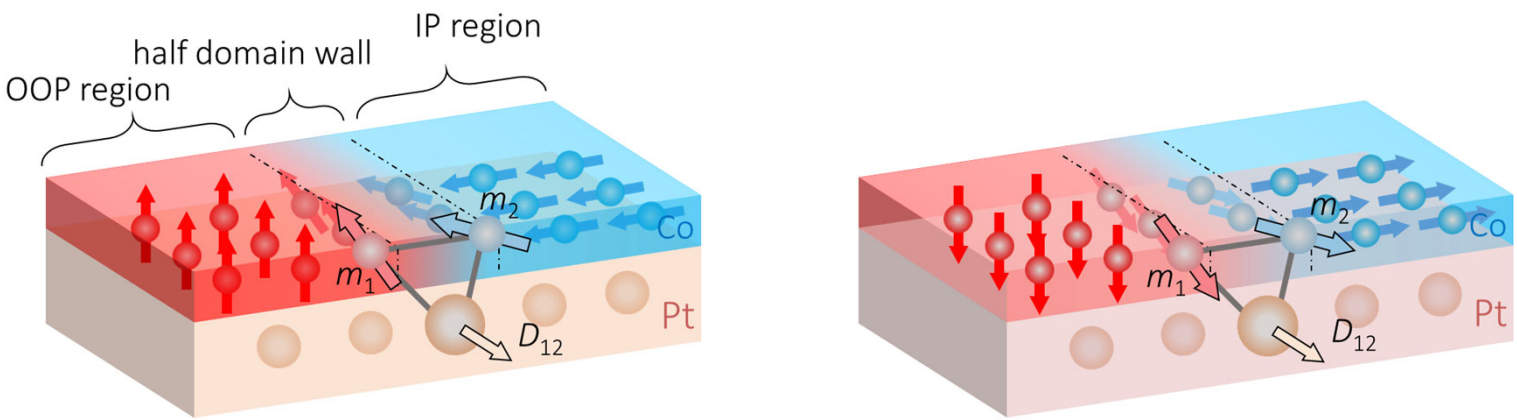
Gating

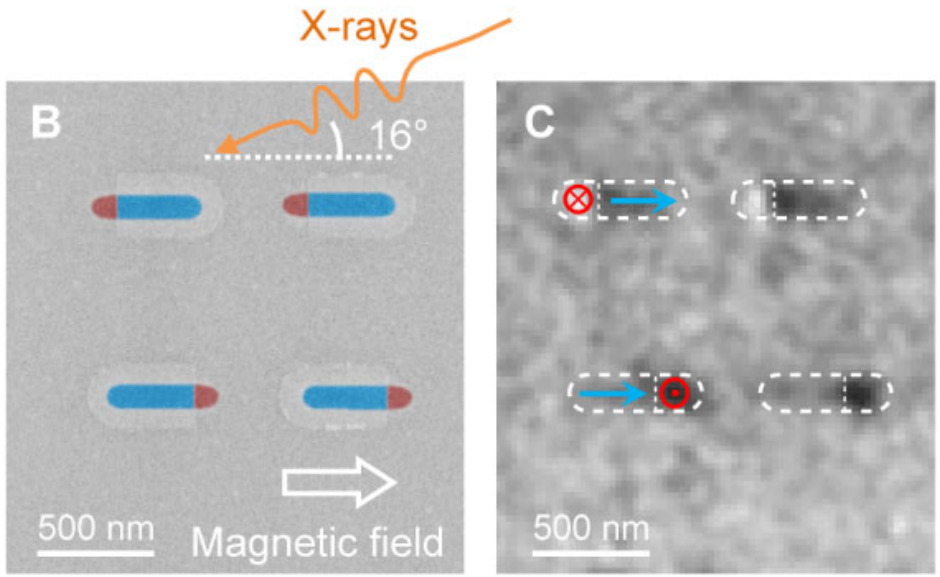
Weisheit et al., Science 2007

Maruyama et al., Nat. Nano. 2009

Bauer et al., Nat. Mater 2013

Chirally coupled OOP and IP nanomagnets

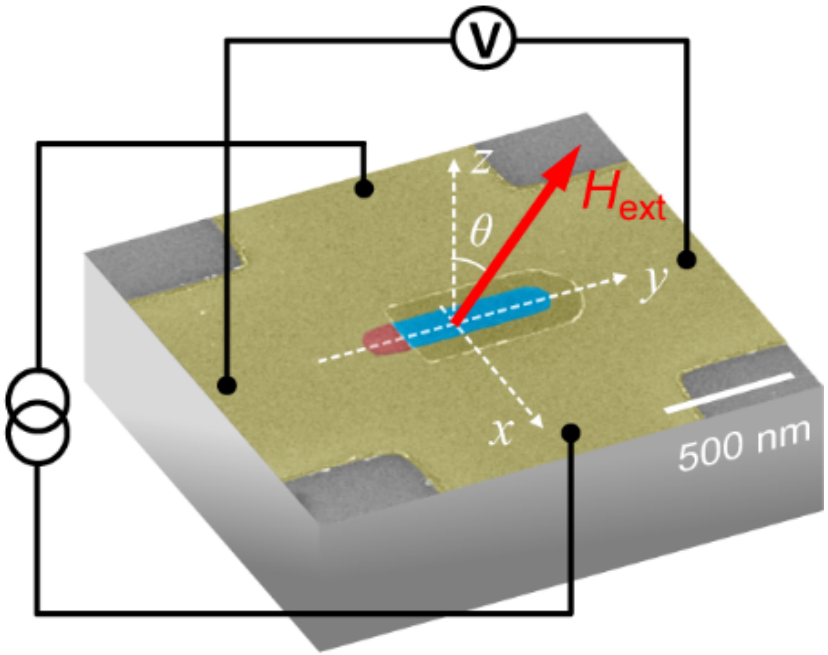


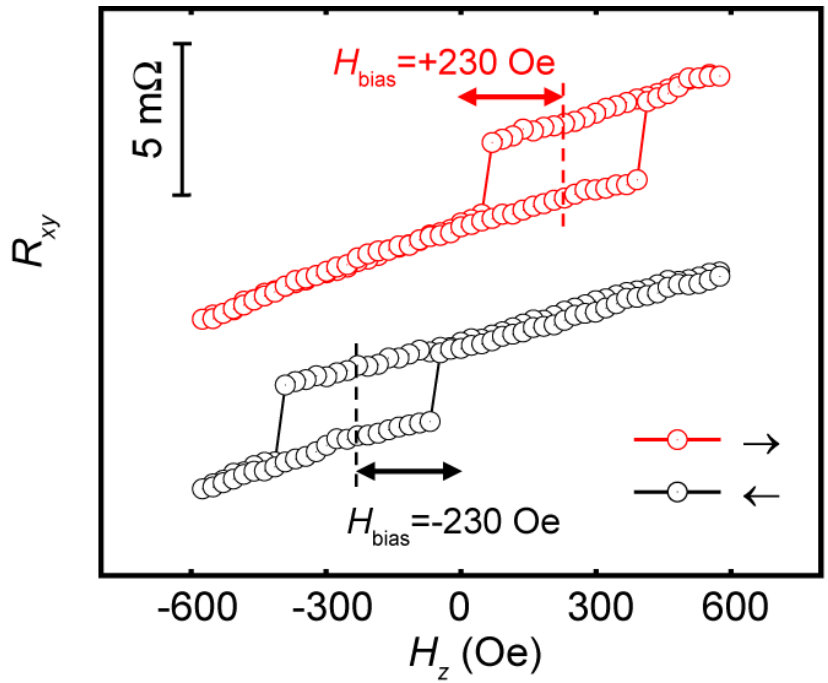


XPEEM @ SIM beamline/PSI

Luo, Dao, Hrabec, Heyderman, PG et al., Science **363**, 1435 (2019)

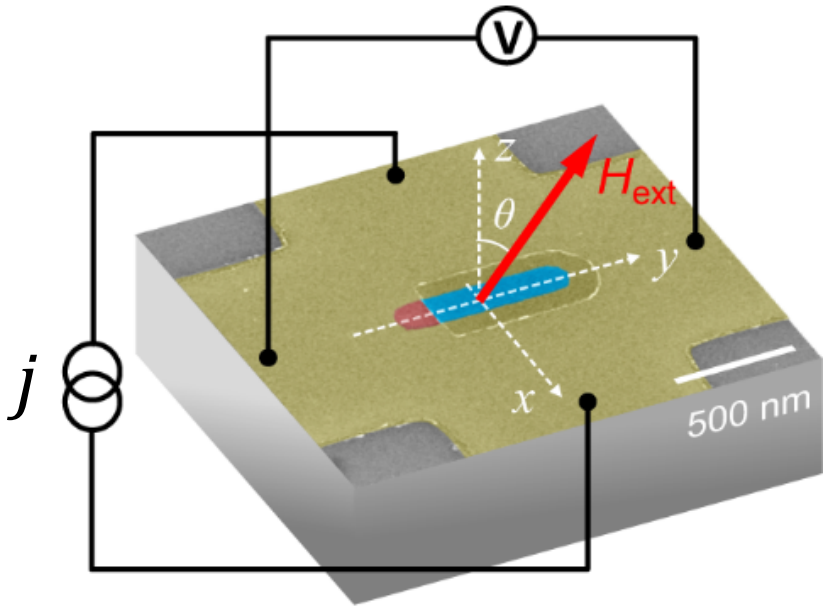
Lateral exchange bias induced by chiral coupling





Luo, Dao, Hrabec, Heyderman, PG et al., Science **363**, 1435 (2019)

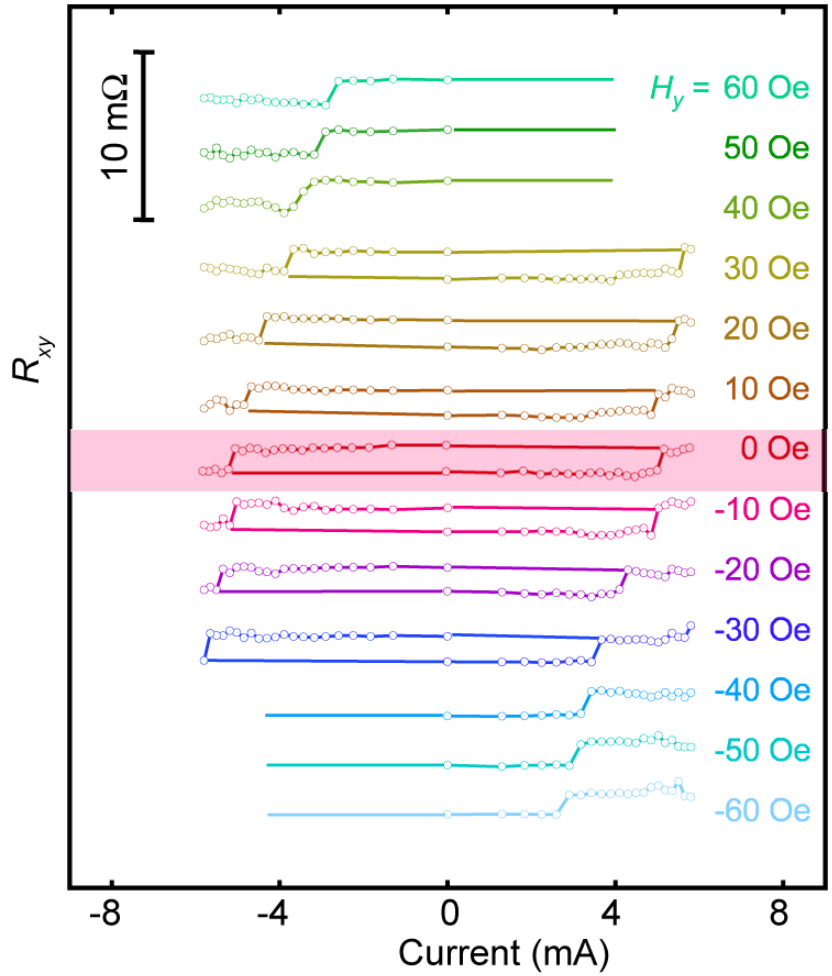
Field-free spin-orbit torque switching of chirally coupled nanomagnets



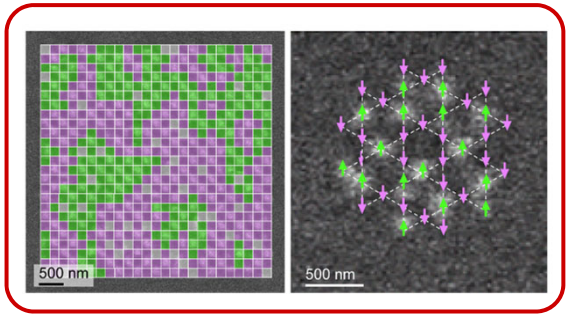
$j \parallel x$

$M_{IP} \parallel y$

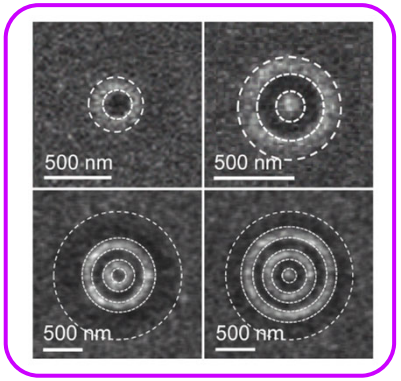
$H = 0$ or $H \parallel y$



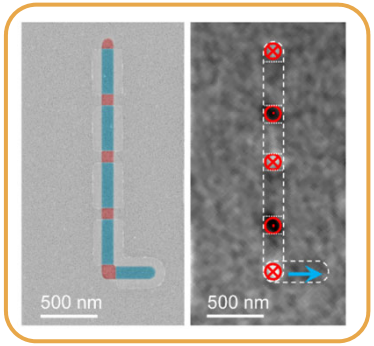
Luo, Dao, Hrabec, Heyderman, PG et al., Science **363**, 1435 (2019)



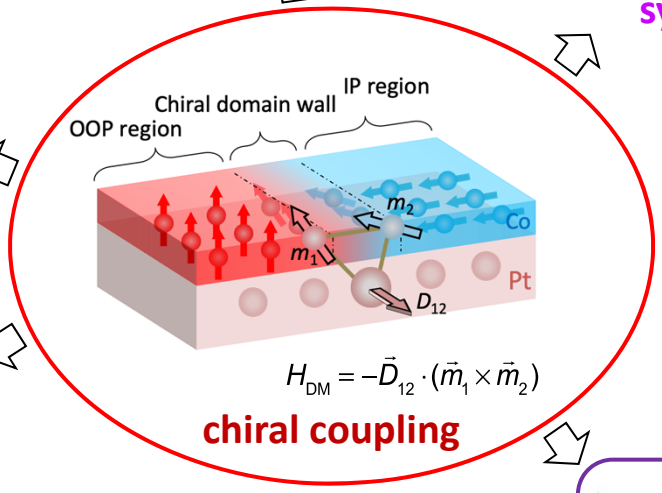
artificial spin ices



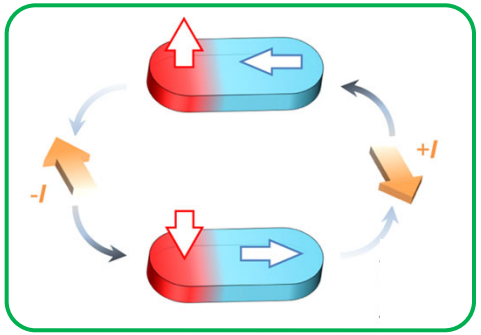
synthetic skyrmions



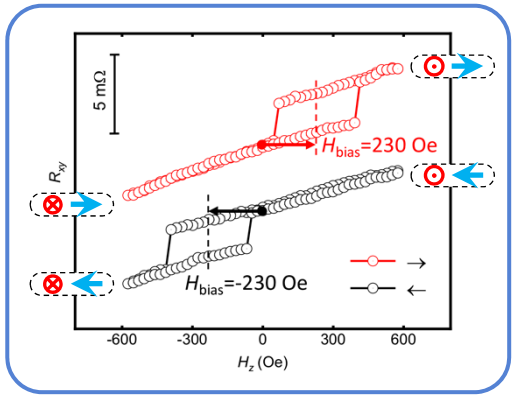
planar synthetic antiferromagnets



chiral coupling



field-free SOT switching



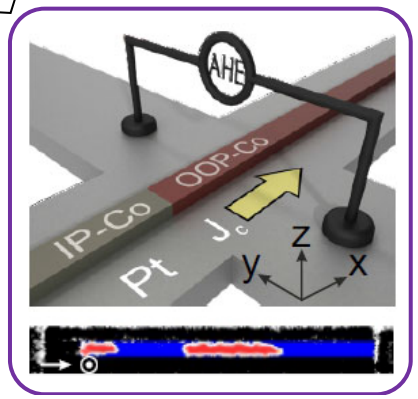
lateral exchange bias

Z. Luo et al.,

Science **363**, 1435 (2019).

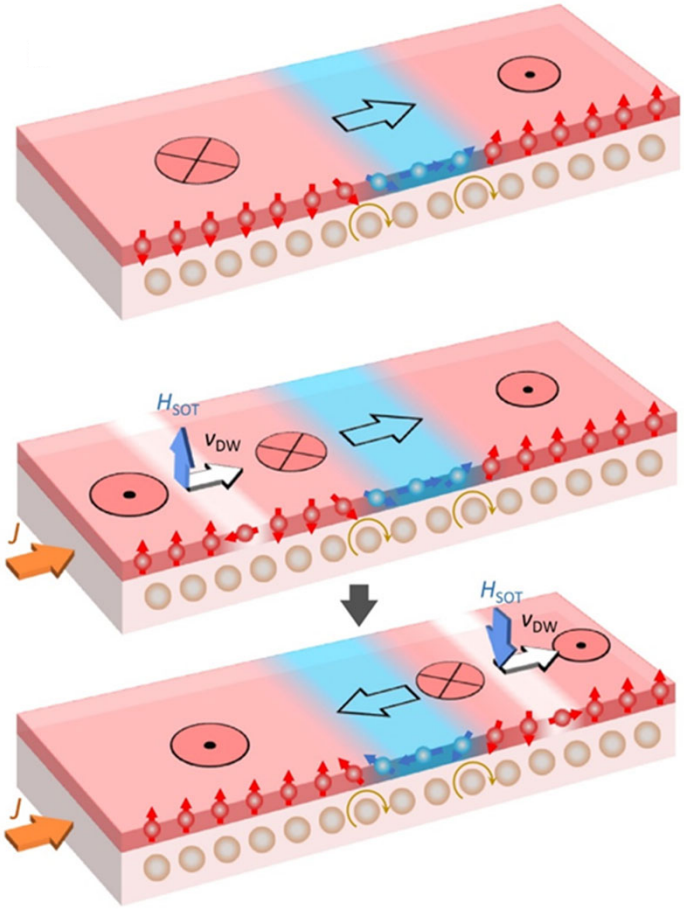
T.P. Dao et al.,

Nano Lett. **19**, 5930 (2019).



domain wall injector

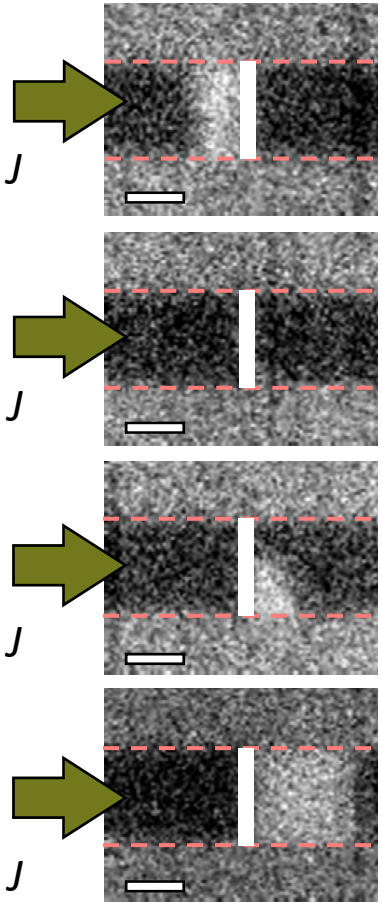
Current-driven domain-wall inverter



Experimental

realization

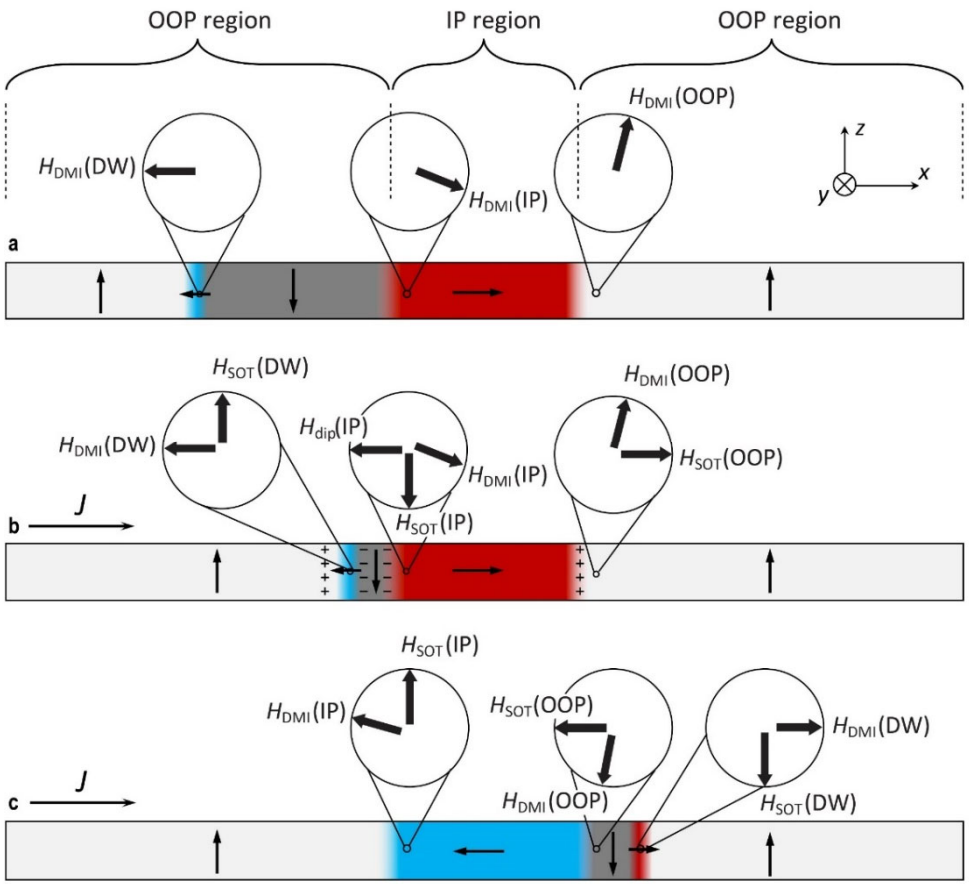
STXM measurement of an OOP-IP-OOP racetrack

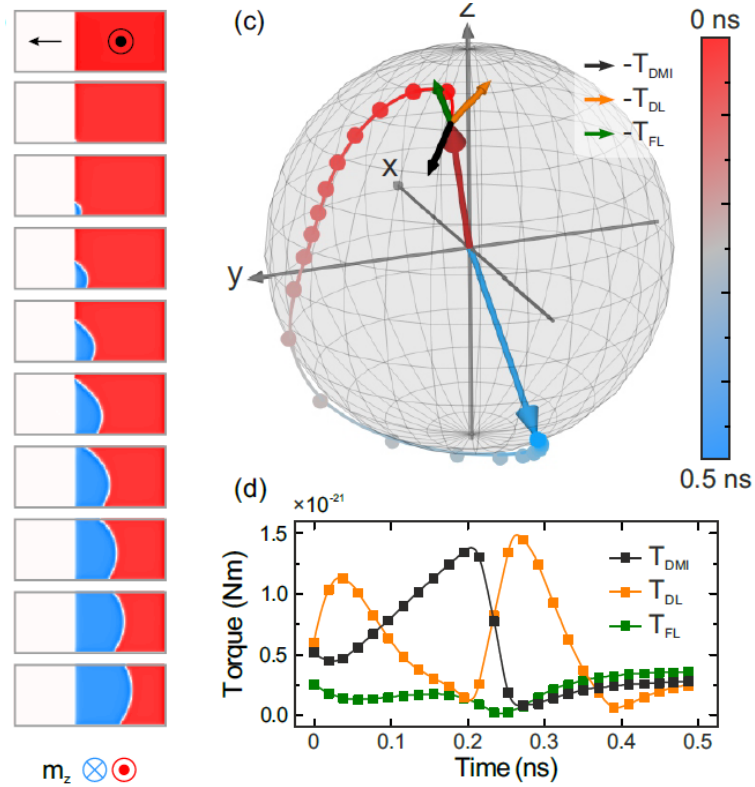


The ⊗|⊙ DW is inverted into a ⊙|⊗ DW by the current pulses

Z. Luo, et al., *Nature* **579**, 214 (2020).

Current-driven domain-wall inversion process

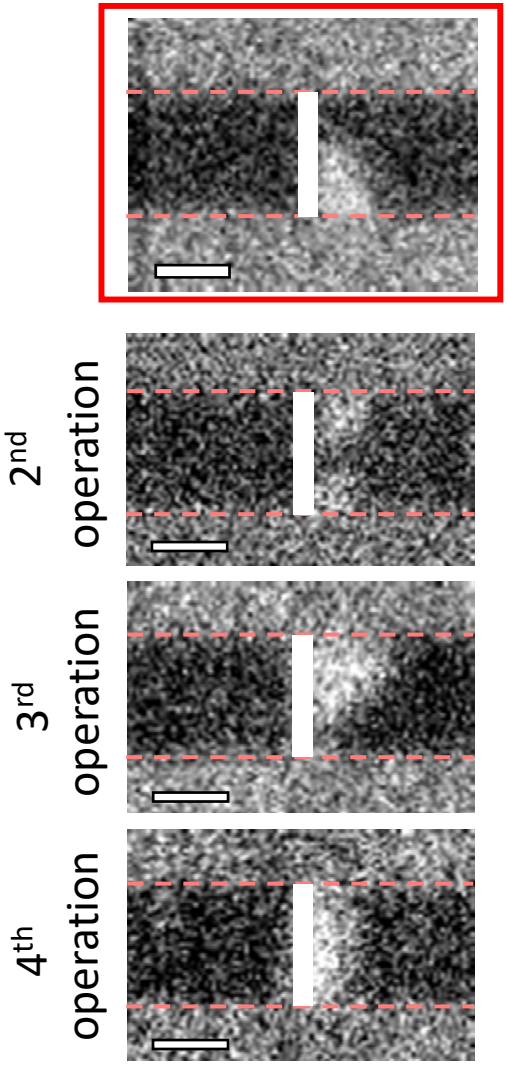




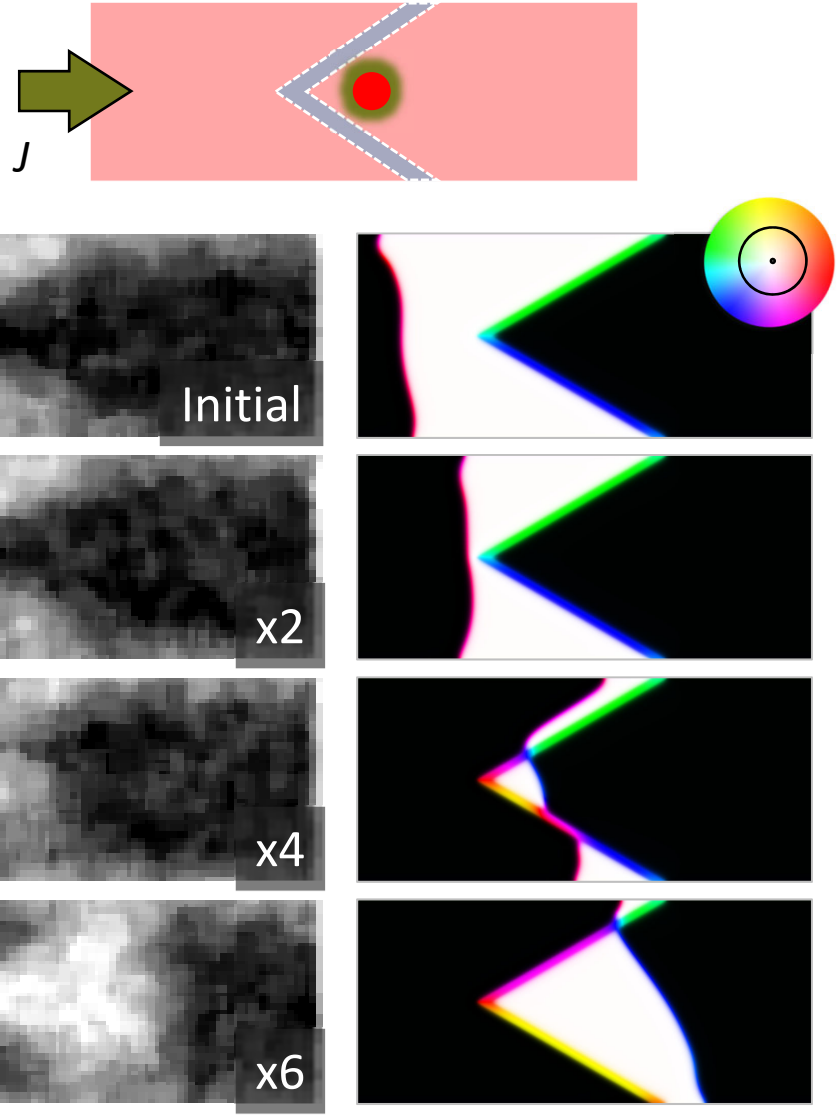
Luo, Hrabec, et al., *Nature* **579**, 214 (2020)

Dao et al., *Nano Lett.* **19**, 5930 (2019)

Nucleation of the reversed domains

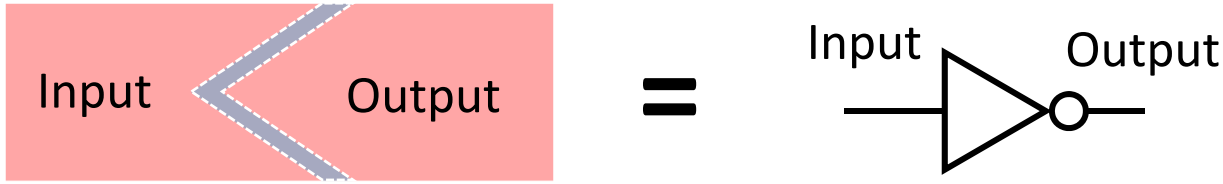


V-shaped IP region provides a well defined nucleation center

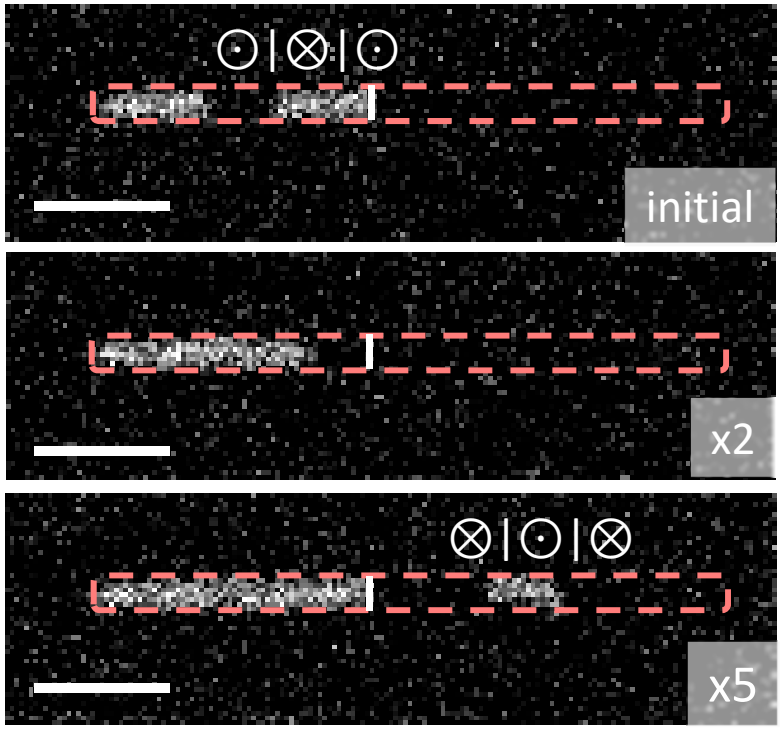


Domain-wall NOT gate

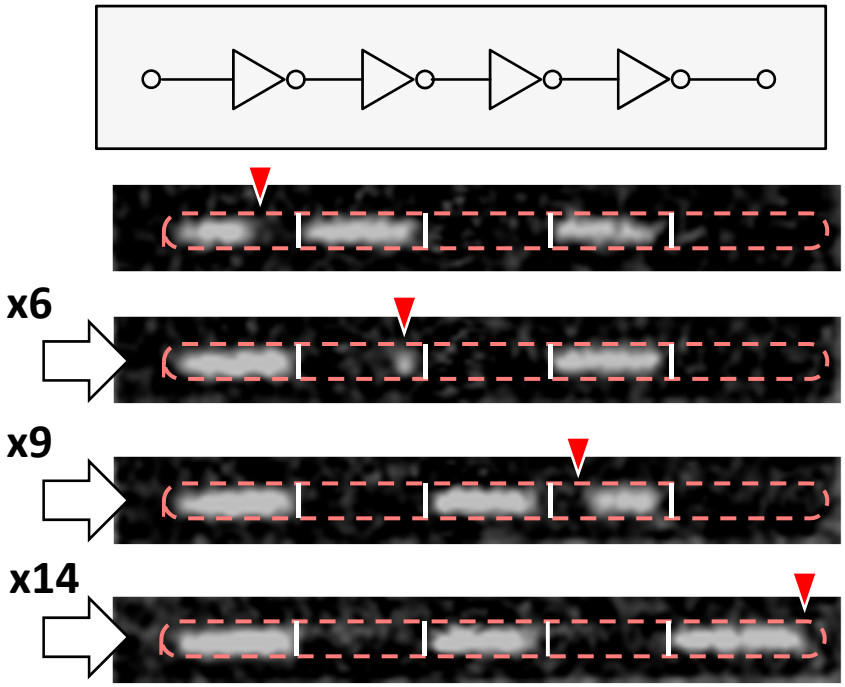
We define ⊗ = logical '1' and ⊙ = logical '0'



Data flow



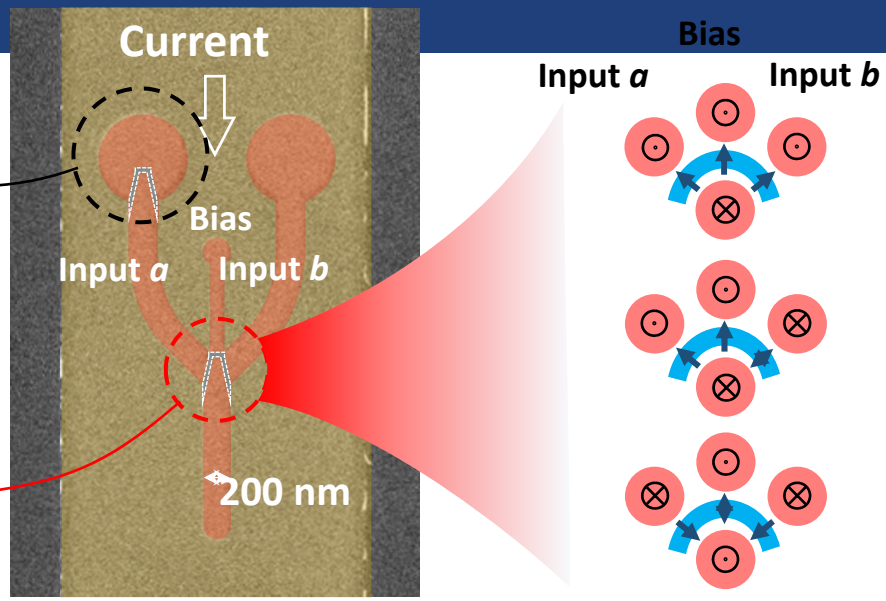
Cascaded NOT gates

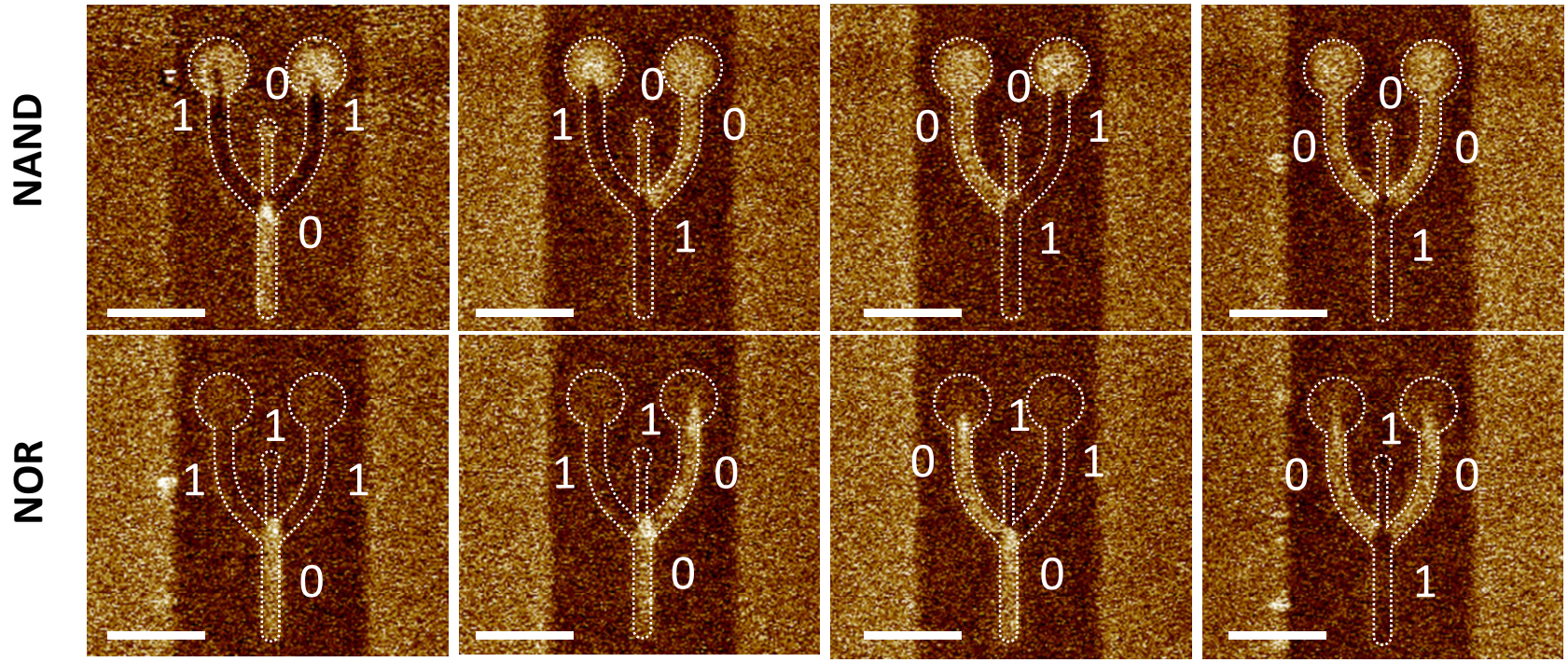


ETH zürich

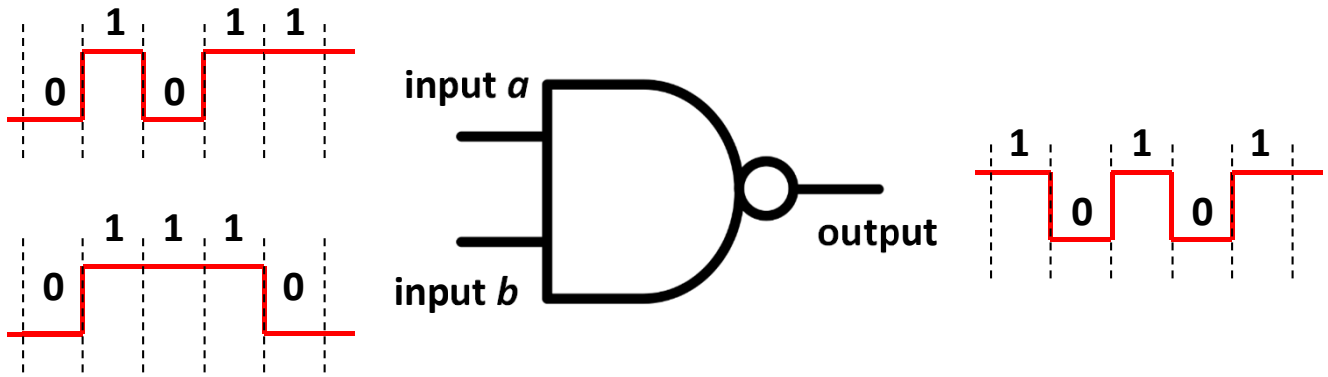
DW reservoir w/wo inverter to define inputs

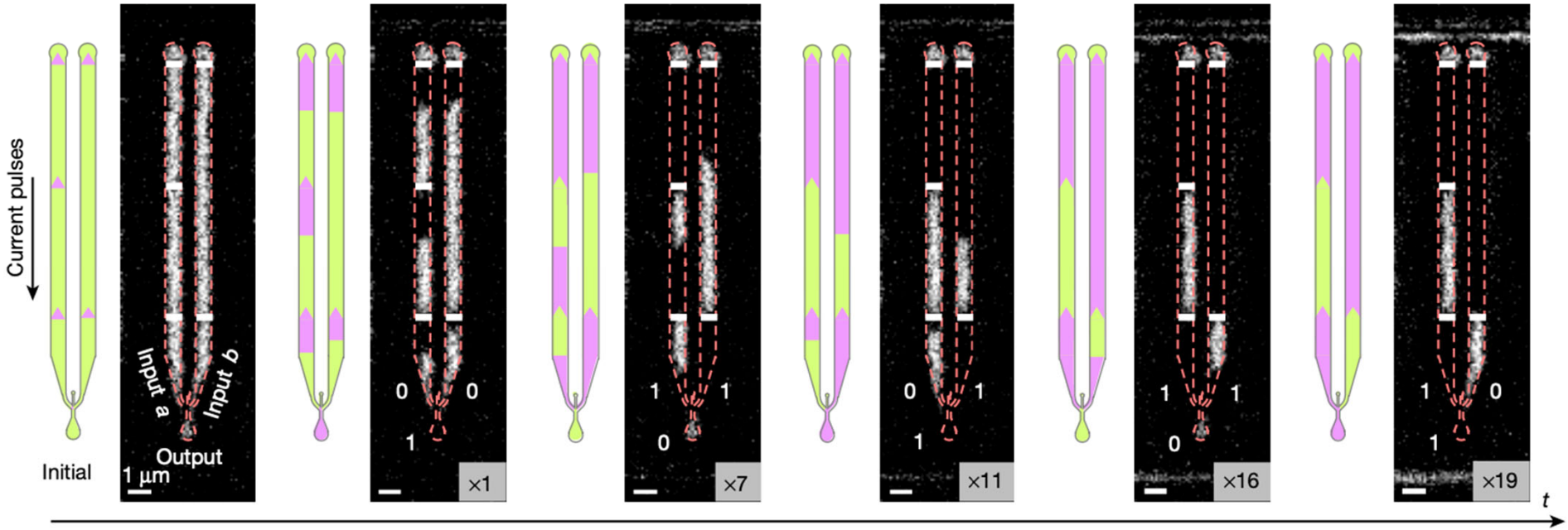
Computation core based on chiral coupling





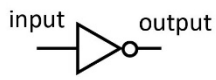
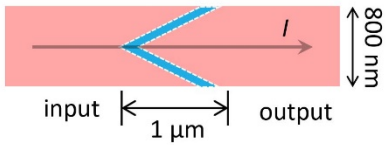
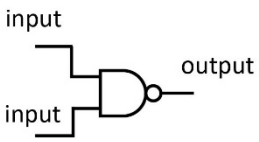
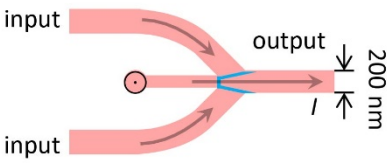
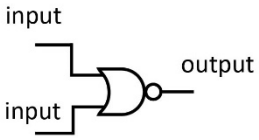
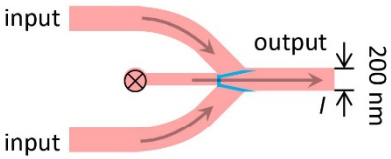
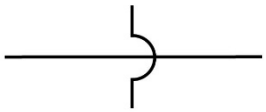
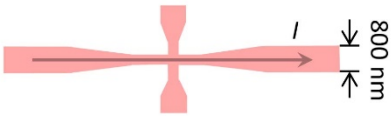
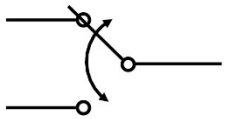
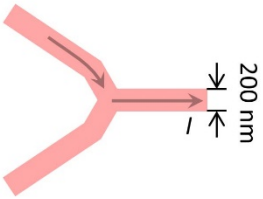
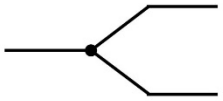
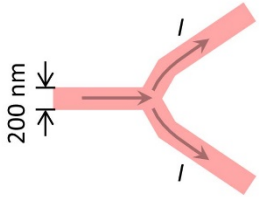
Current-driven operation of a NAND gate with a sequence of logic inputs

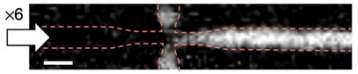


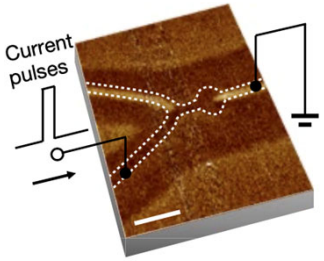


Luo, Hrabec, et al., *Nature* **579**, 214 (2020)

A complete set of logic elements

Symbol	Magnetic DW logic
 NOT gate	
 NAND gate	
 NOR gate	
 Cross-over	
 Switch	
 Fan-out	



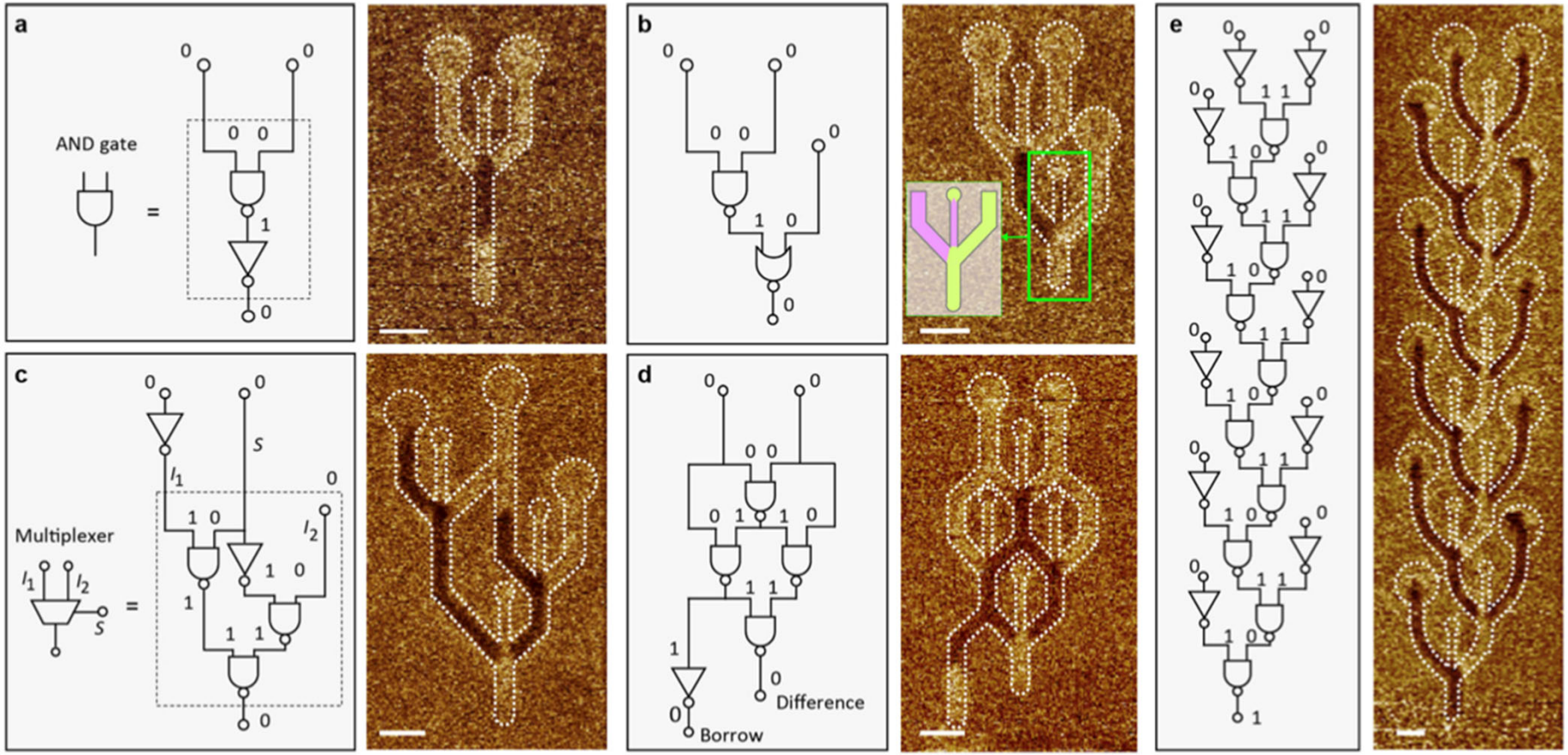


Luo, Hrabec, et al.,

Nature **579**, 214 (2020)

Examples of DW logic circuits #1

AND gate **NAND+NOR circuit**

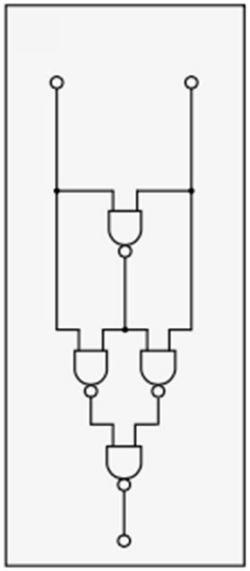


2-bit multiplexer **Half subtractor** **Long circuit**

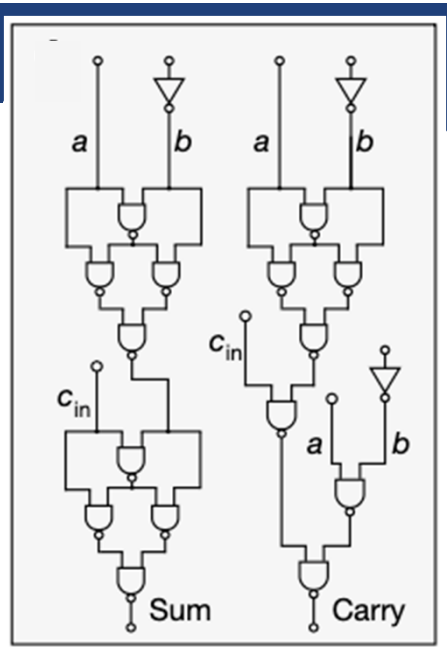
Luo, Hrabec, et al., *Nature* **579**, 214 (2020)

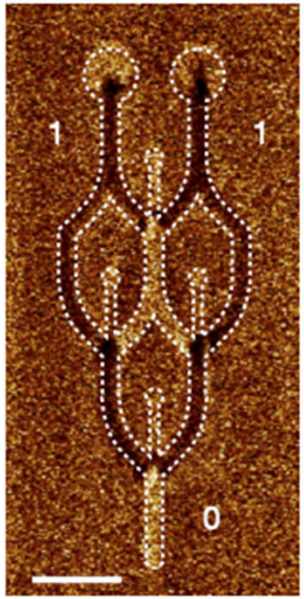
Examples of DW logic circuits #2

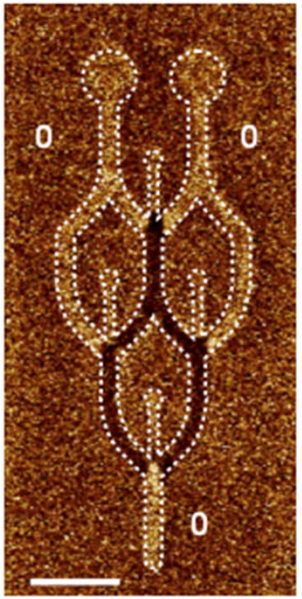
Half adder

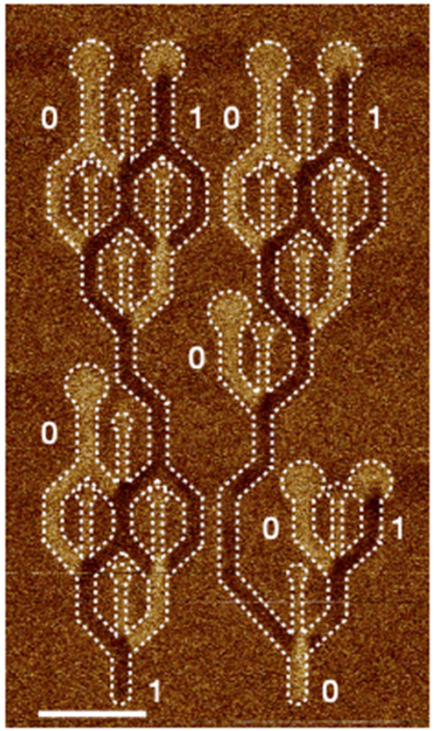


Full adder

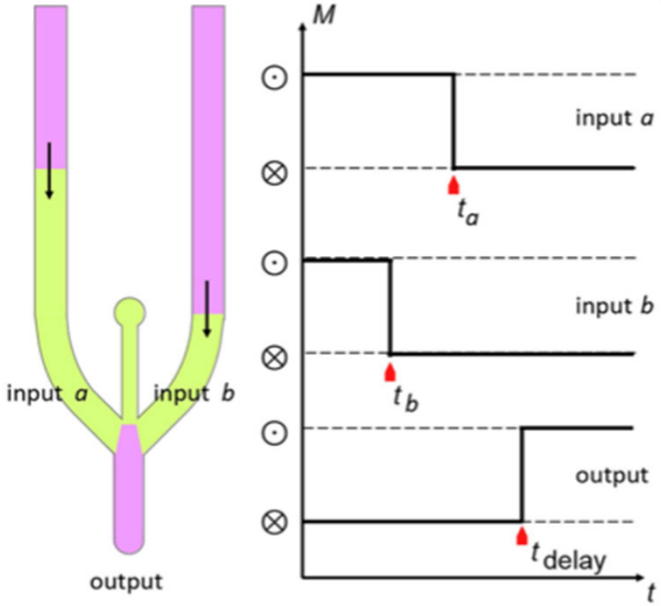


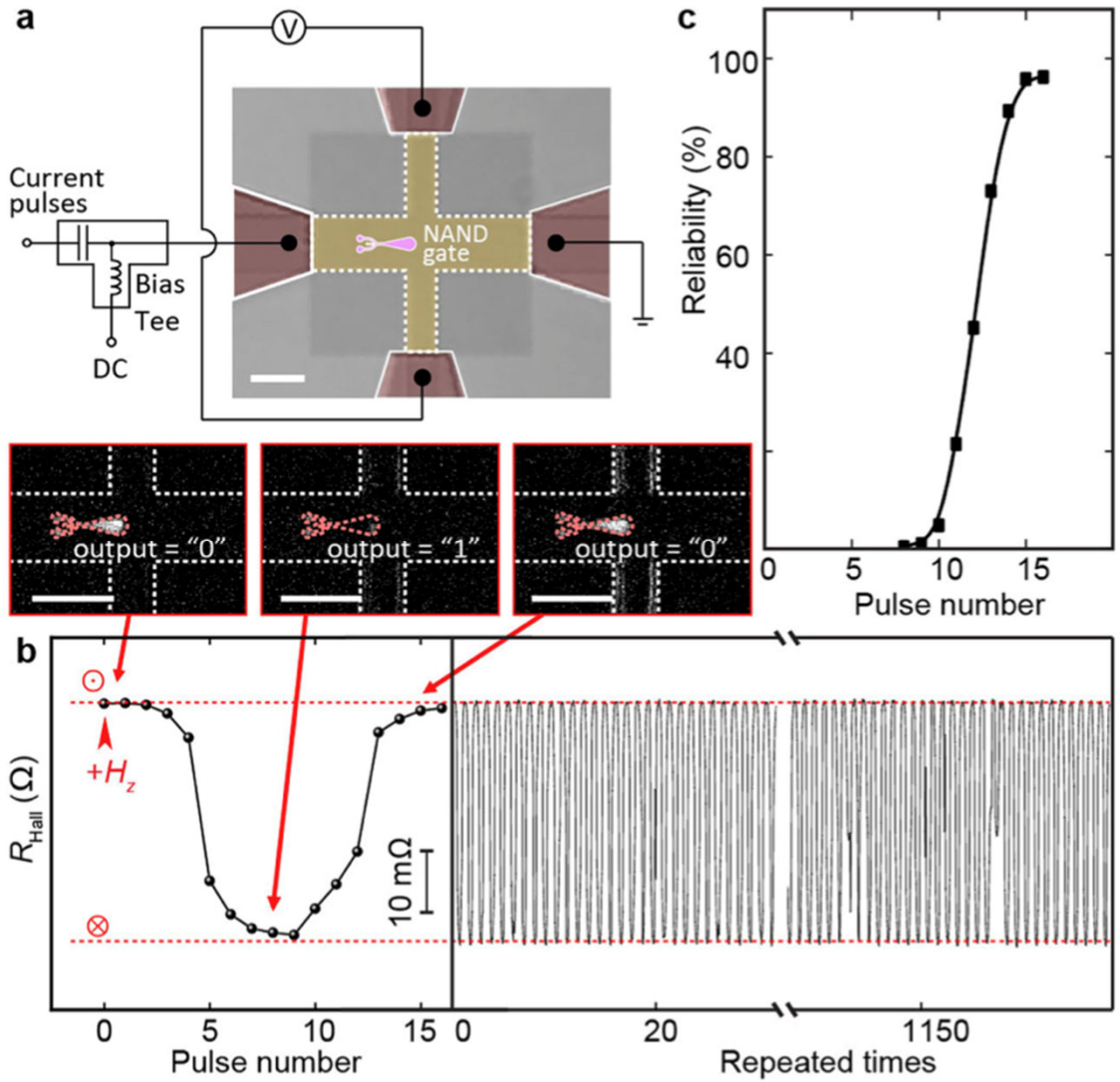






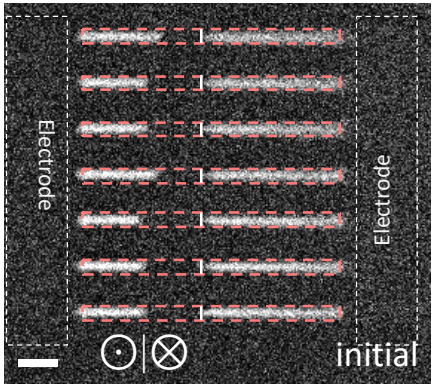
Propagation delay time for DW motion





- Asynchronized DW motion
- Need for delay time

Issues to be addressed in the future

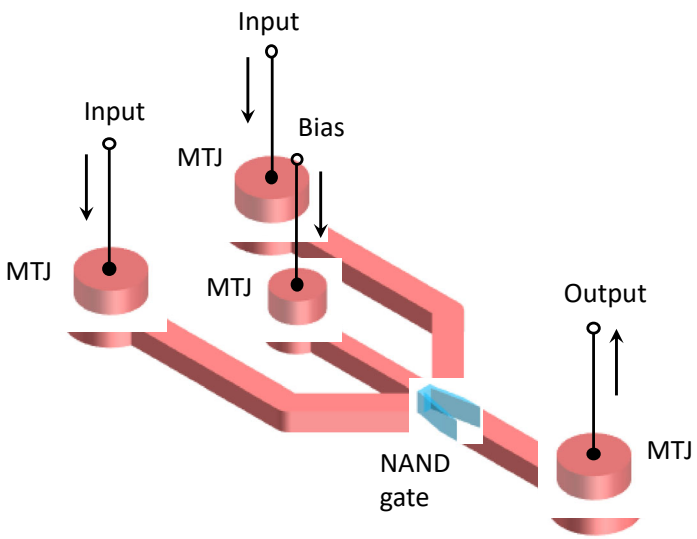


800 nm-wide DW inverter ~150 m/s →

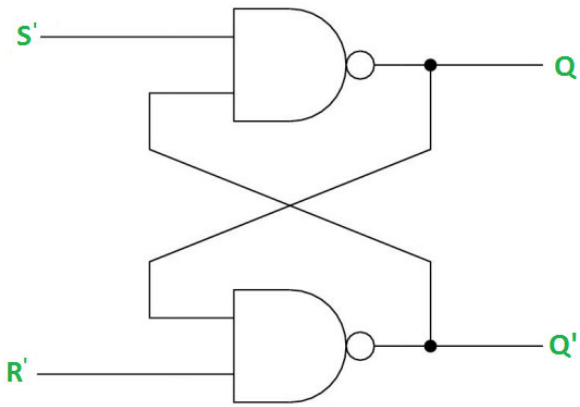
Scaling down vs performances

- Pinning
- DW speed
- Synchronization

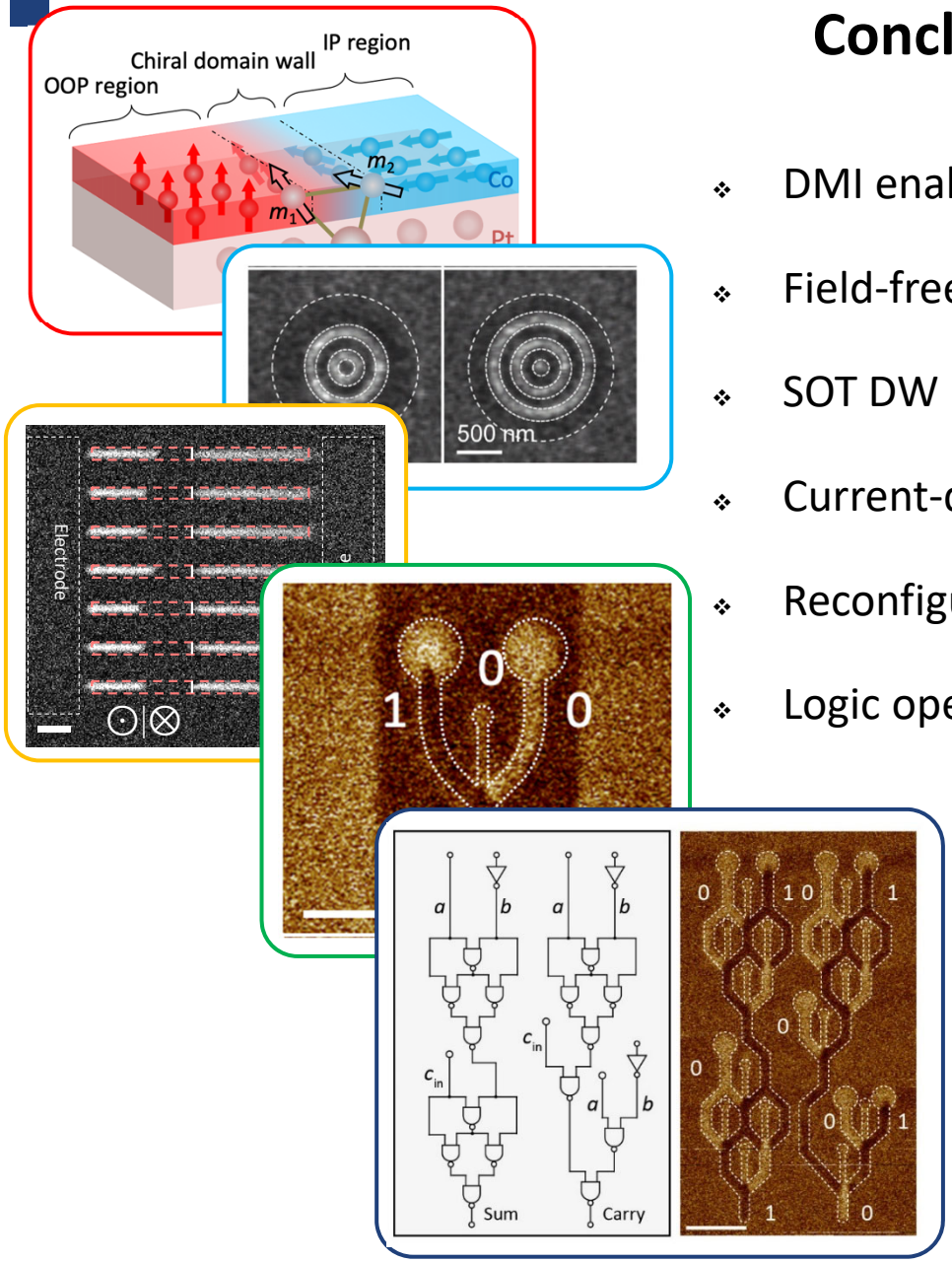
Integration



Feedback loops



Conclusions #2



- DMI enables flexible design of synthetic chiral magnets
- Field-free switching in OOP-IP coupled magnets
- SOT DW injectors
- Current-driven DW inverter
- Reconfigurable NAND/NOR gate
- Logic operations with DWs in cascaded logic circuits

Z. Luo, et al., *Science* 363, 1435 (2019).

T.P. Dao, et al., *Nano Lett.* 19, 5930 (2019).

Z. Luo, et al., *Nature* 579, 214 (2020).

Z. Luo, et al., EU patent EP20161352.8.