Spintronics Nanodevice
- How small can we make it and what else can we use it for -

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Outline

1. What spintronics delivers

2. Scaling further

3. Can you do more

Current Working Memories

DRAM: dense, $6F^2$

SRAM: fast, $200F^2$

Volatile

Energy Consumption & Carbon Footprint of the IT Sector

ICTFOOTPRINT.EU

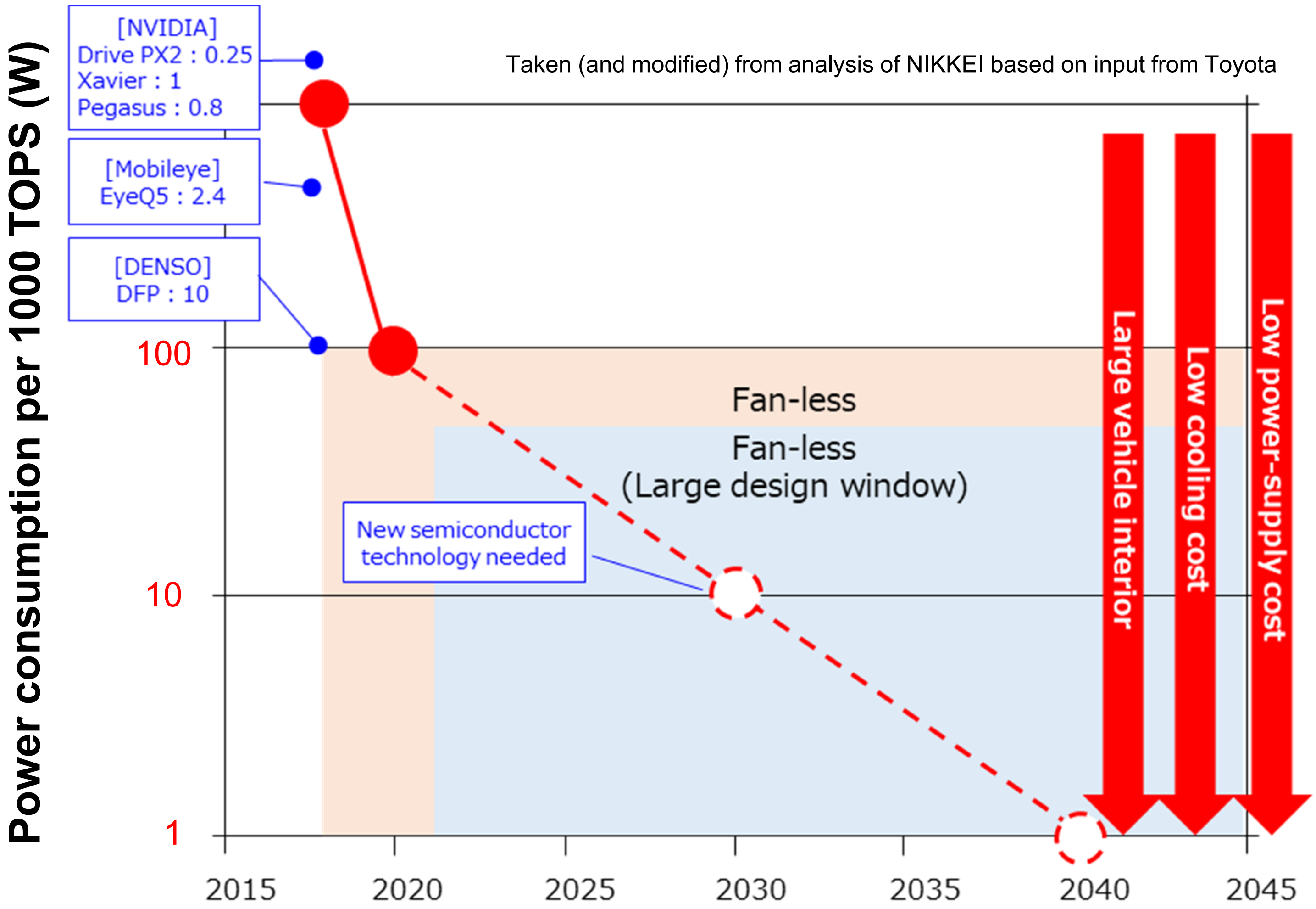
Wednesday, July 18, 2018

Internet-connected devices produce 3.5% of global emissions within 10 years and 14% by 2040. (Source: Climate Home News)

Communications industry responsible for 20% of all the world's electricity in 2025. (Source: The Guardian)

Data centers consume 1/5 of Earth's power in 2025. (Source: Data Economy).

AI chip requirement for autonomous driving



http://archive.doobybrain.com/2013/09/03/office-building-lights-night/

Announcements of STT-MRAM 2017-2018

SAMSUNG

Samsung ready to mass produce MRAM chips

28nm FD-SOI process

Samsung Foundry will soon be ready to enter mass production of magnetoresistive random-access memory (MRAM) chips built using 28nm fully depleted silicon-on-insulator (FD-SOI) process technology, according to Korea media reports.

Digitimes, 26 Sep. 2017.

tsmc

TSMC to start eMRAM production in 2018

22 nm process

According to re… embedded MRA… reception. …iming to start producing …duction" to gauge market

MRAM-info, 8 Jun. 2017.

GLOBALFOUNDRIES

GLOBALFOUNDRIES Announces Availability of Embedded MRAM on Leading 22FDX® FD-SOI Platform

Sep 20, 2017

Advanced embedded non-vol… the 22nm process node

22nm FD-SOI

Santa Clara, Calif., Septemb… …bedded magnetoresistive non-volatile memory (eMRAM) technolog… …mbedded memory solution, GF's 22FDX eMRAM provides high performance and superior reliability for broad applications in consumer and industrial controllers, data centers, Internet of Things (IoT), and automotive.

GLOBALFOUNDRIES press release, 20 Sep. 2017.

intel

Intel says its embedded 22nm MRAM is production ready

22nm FinFET CMOS

In Octobe… integrated… …e company has successfully …wafers.

MRAM-info, 20 Feb. 2019.

MTJ Size ～ several 10 nm

Papers presented at IEDM2019

TOHOKU UNIVERSITY

EVERSPIN TECHNOLOGIES — Demonstration of a Reliable 1 Gb Standalone Spin-Transfer Torque MRAM For Industrial Applications

SAMSUNG — 1Gbit High Density Embedded STT-MRAM in 28nm FDSOI Technology

GLOBALFOUNDRIES — Manufacturable 22nm FD-SOI Embedded MRAM Technology for Industrial-grade MCU and IOT Applications

intel — 2 MB Array-Level Demonstration of STT-MRAM Process and Performance Towards L4 Cache Applications

tsmc — 22nm STT-MRAM for Reflow and Automotive Uses with High Yield, Reliability, and Magnetic Immunity and with Performance and Shielding Options

Nonvolatile spintronic device - Magnetic Tunnel Junction -

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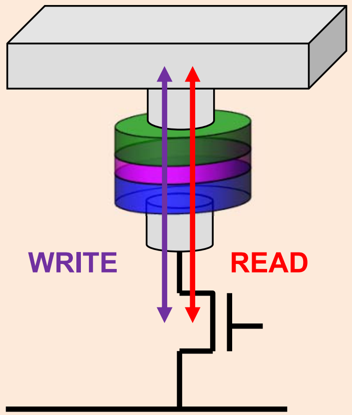
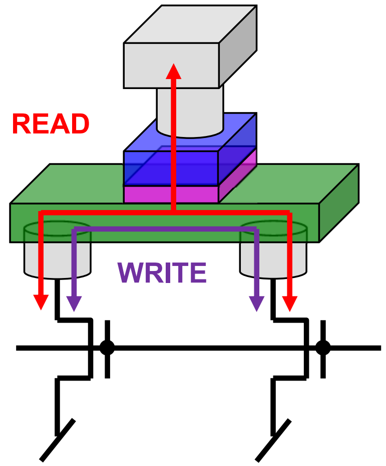
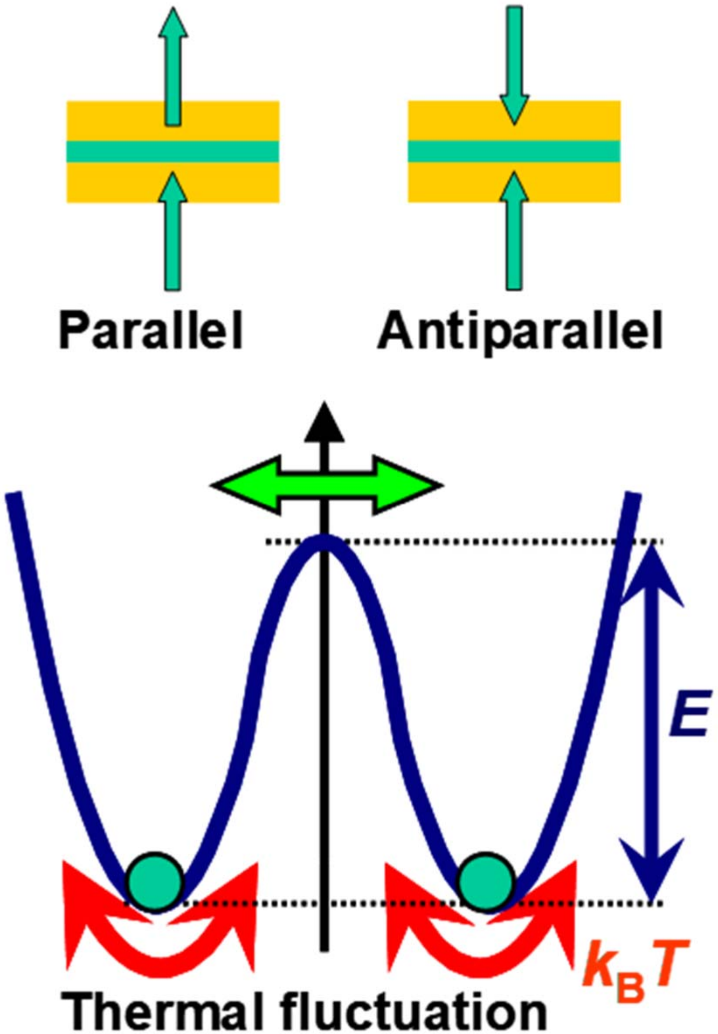
	Two-terminal	**Three-terminal**
Structure		
Application	• Large capacity	• High-speed, high-reliability
Switching	• **Spin-transfer torque (STT)** • Electric field	• Current-induced DW motion • **Spin-orbit torque (SOT)**



$$\tau = \tau_0 e^{E/k_B T}$$

$E/k_\mathrm{B}T > 80$

Perpendicular to the plane

Switching efficiency

Footprint

Energy barrier E

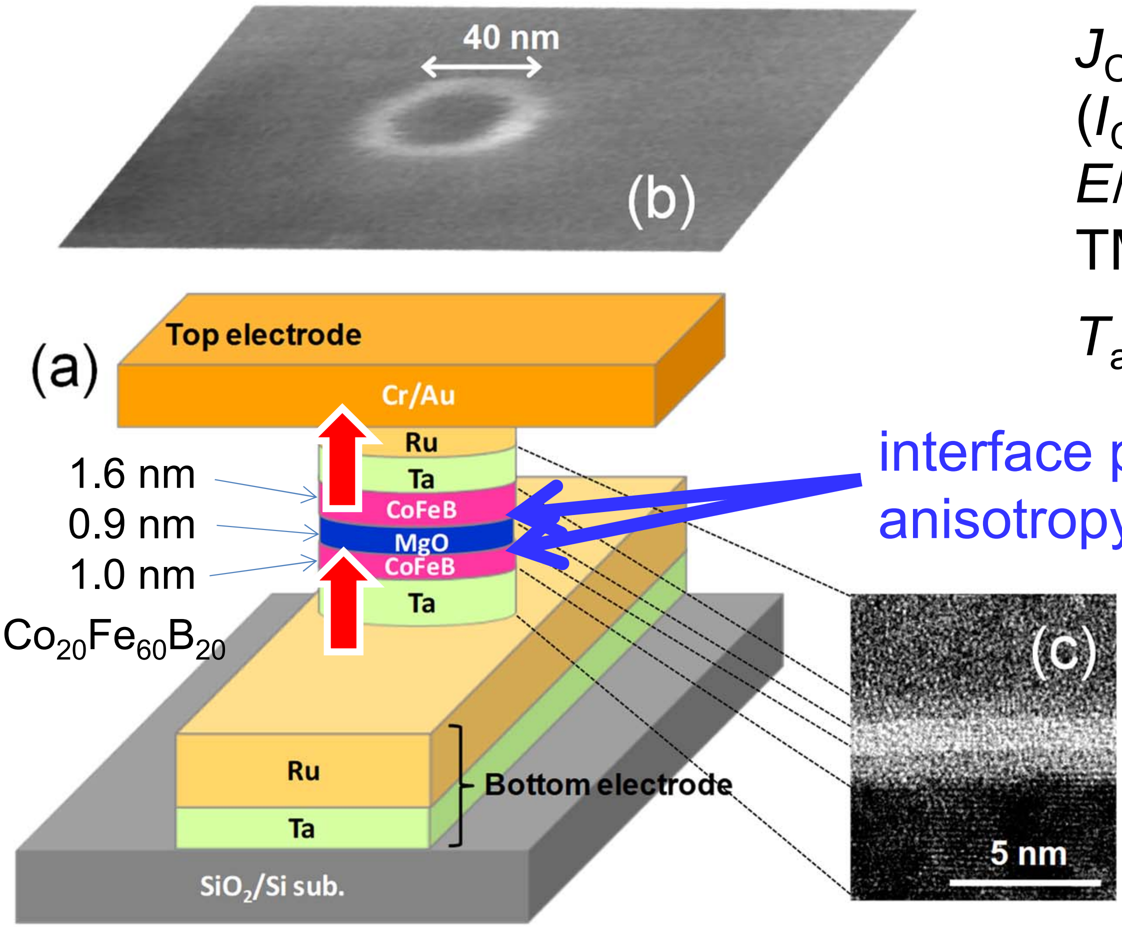
$$E = N \frac{M_S^2}{2\mu_0} V + K_i S$$

V: volume
S: area

shape anisotropy

interface anisotropy

Perpendicular MgO-CoFeB Magnetic Tunnel Junction



J_{C0} = 3.8 MA/cm^2
(I_{C0} = 48 μA)
E/k_BT ~ 40
TMR ratio = 110%
T_a = 350°C **now > 400°C**

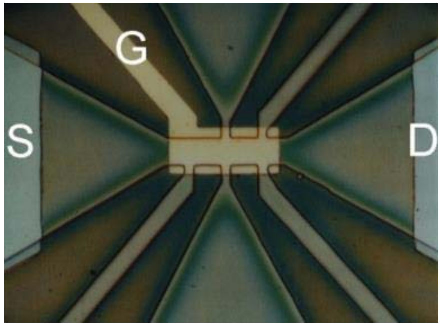
interface perpendicular anisotropy

$$E = -\frac{M_S^2}{2\mu_0}V + K_i S$$

S. Ikeda *et al.*, *Nature Mat.* **9**, 721 (2010)

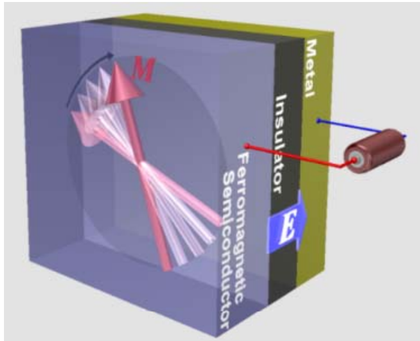
Electric-field control of magnets

Ferromagnetic transition and coercivity

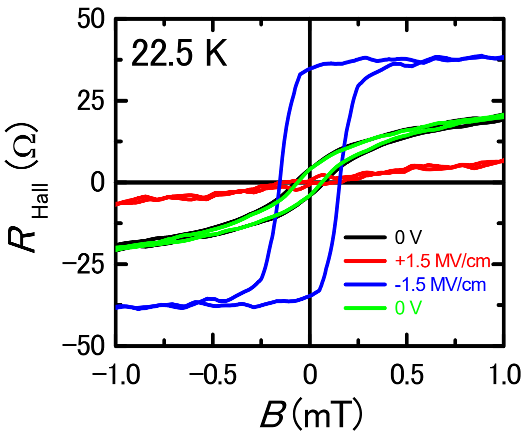


Ferromagnetic semiconductor (In,Mn)As

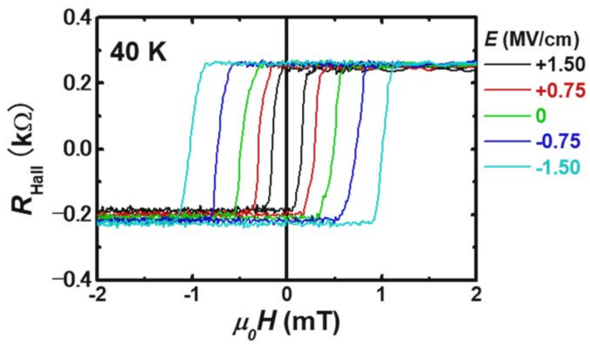
Magnetization direction



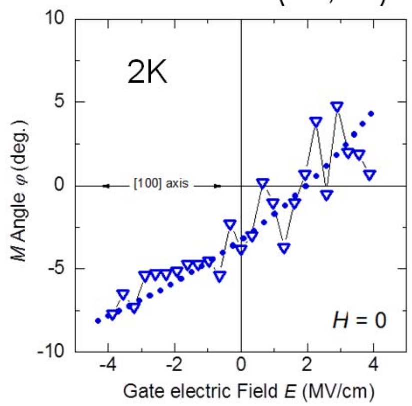
Ferromagnetic Semiconductor (Ga,Mn)As



H. Ohno *et al.*, *Nature* 408, 944 (2000)

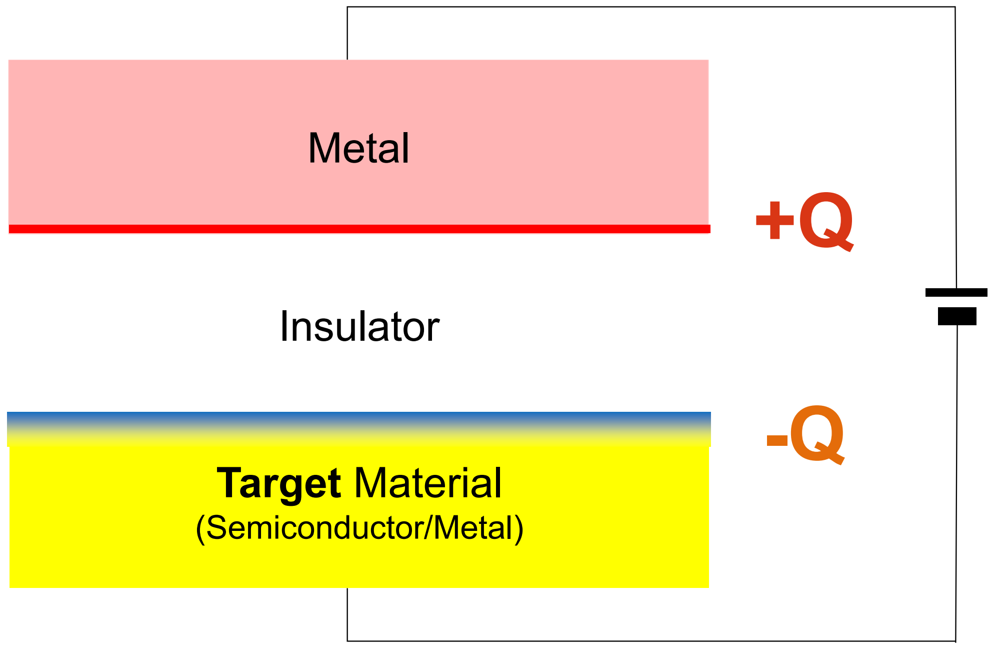


D. Chiba *et al.*, *Science* 301, 943 (2003)

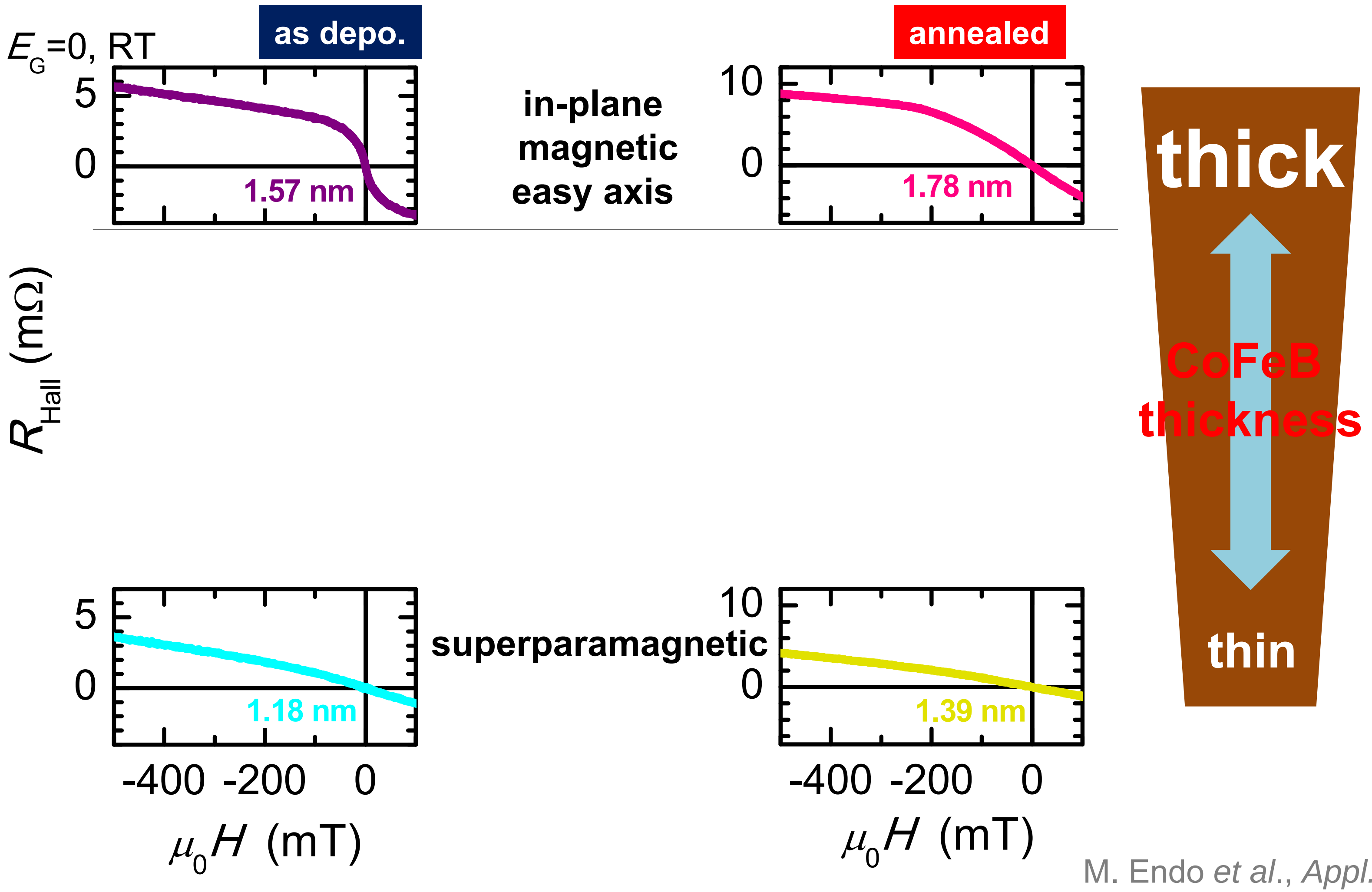


D. Chiba *et al.*, *Nature* 455, 515 (2008)

Electric-field control

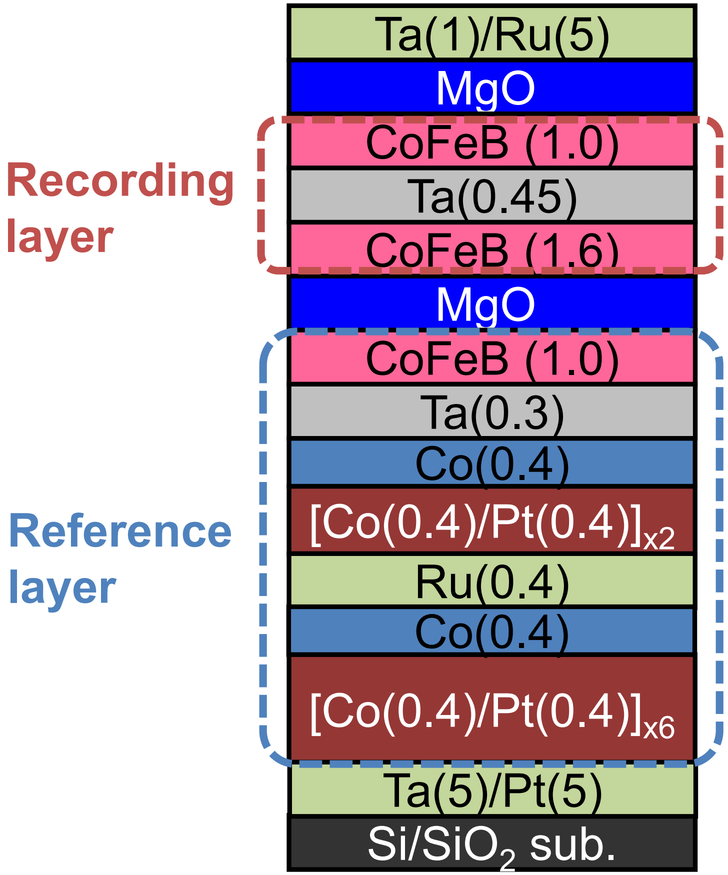


Thickness dependence of anisotropy in CoFeB/MgO



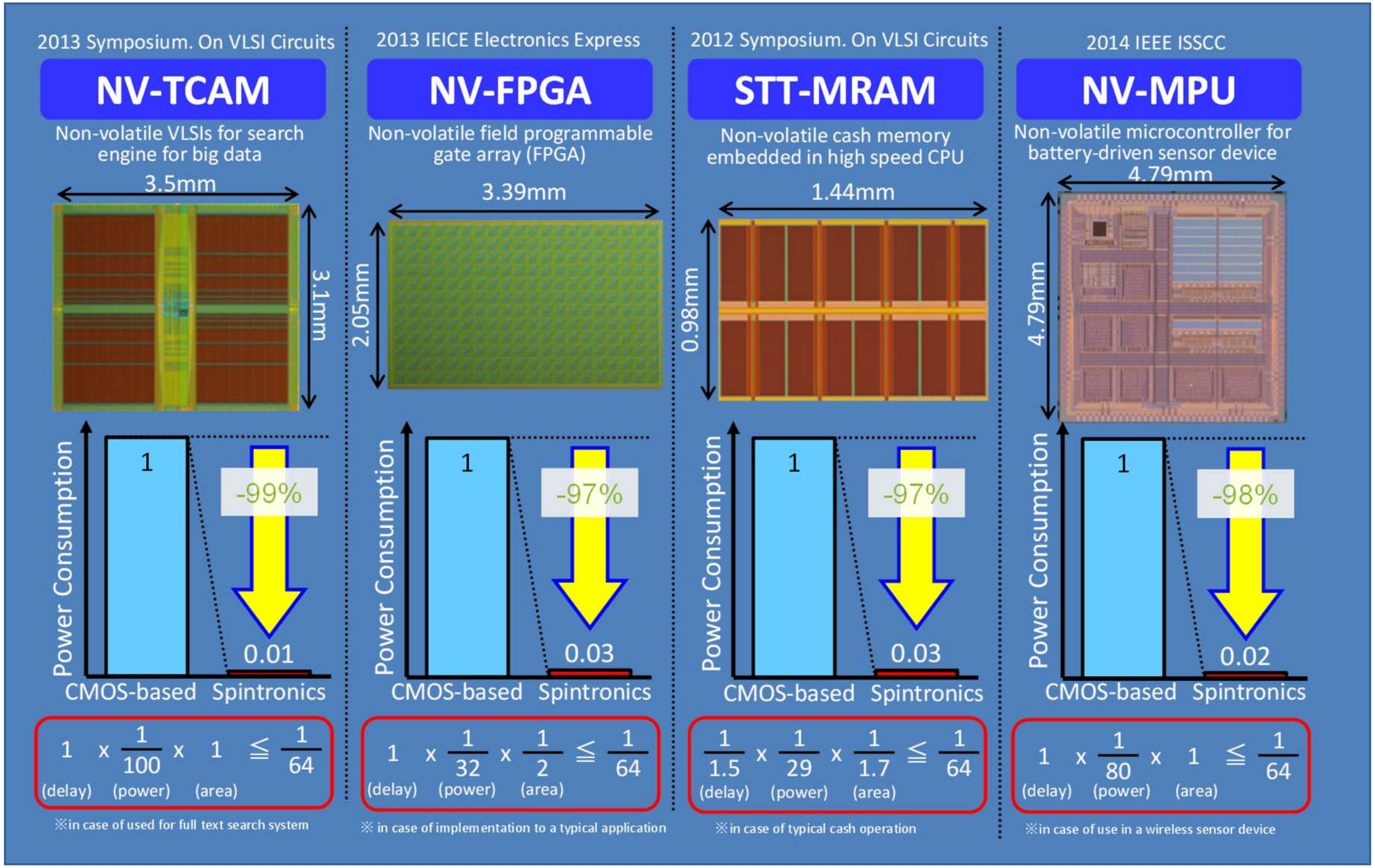
M. Endo *et al.*, *Appl. Phys. Lett.* (2010)

Double CoFeB-MgO interface structure



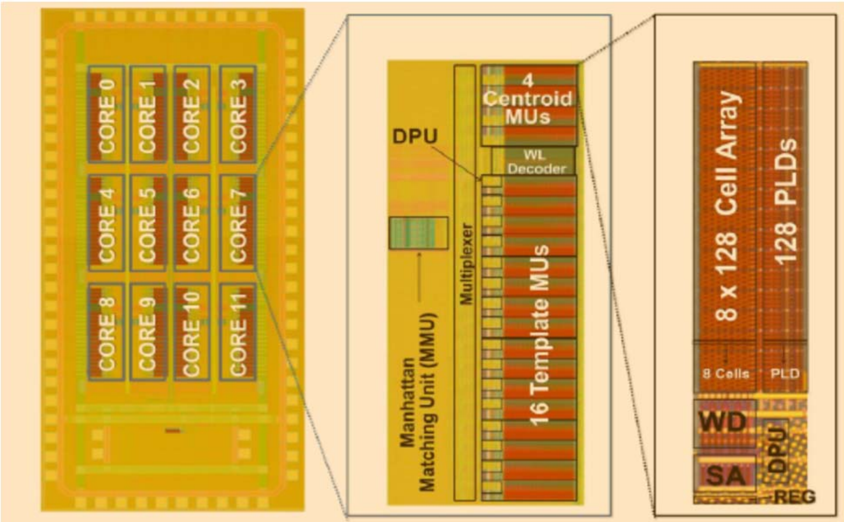
H. Sato and HO *et al*., Appl. Phys. Lett. **105**, 062403 (2014).

MTJ/CMOS Low Power VLSIs



Prototype on 300 mm by Tohoku University

AI Processor by CMOS/MTJ VLSI



(a) Prototype Chip [proposed processor] (b) Processor Core (c) MU

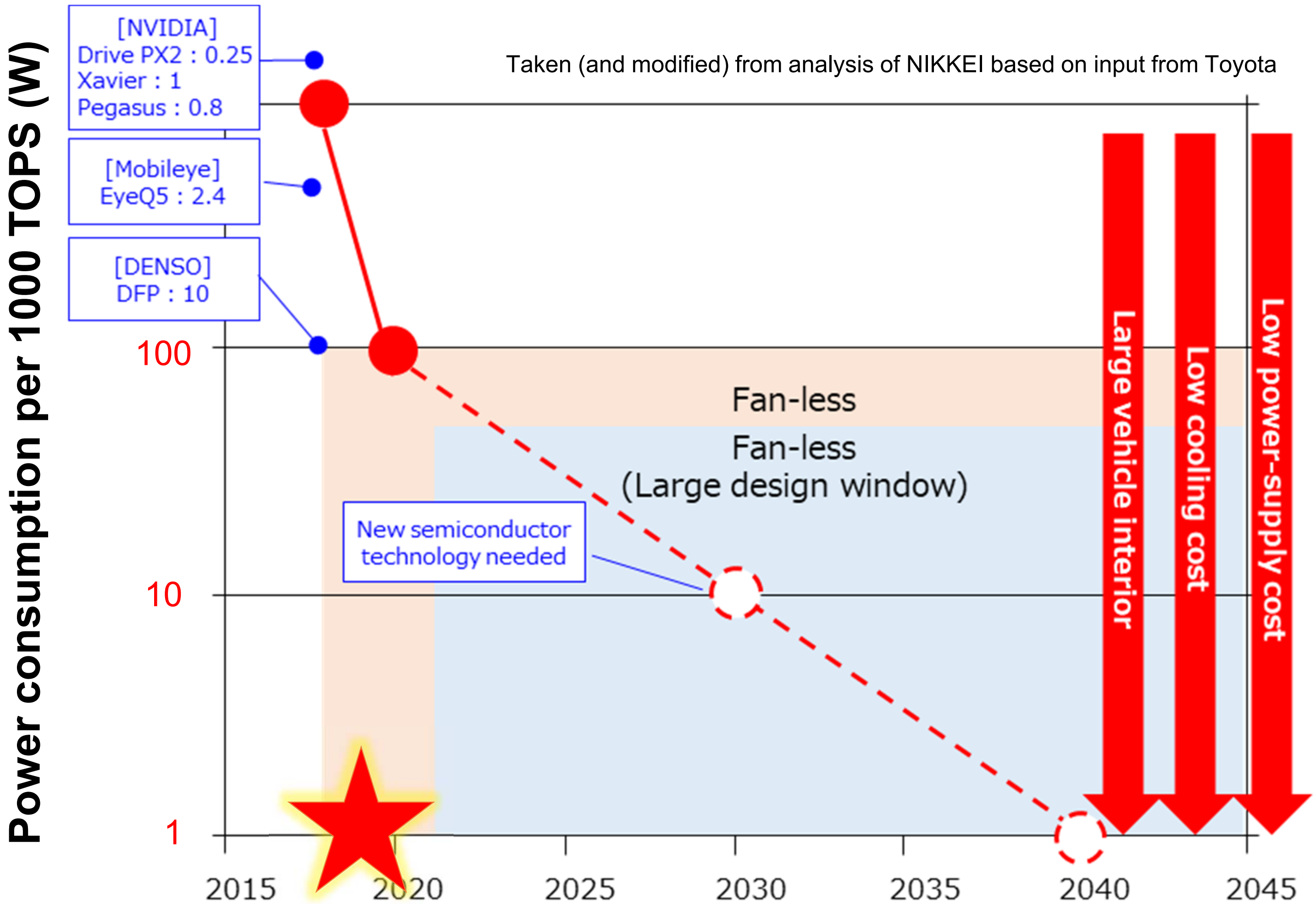
Associative processor includes **12 core unit processor**.

Process	90nm-CMOS/70nm-MTJ
Core Size	0.3mm x 0.9mm
Frequency	20 MHz
Supply Voltage	0.9 V
Average Operation Power	**600 μW** **(30μW/MHz)**
Throughput (cycles/vector)	16

Y. Ma *et al.* Jpn. J. Appl. Phys. **55** 04EF15 (2016).

Tensor Processing Unit（TPU）＠Google
- Process: 28 nm CMOS
- Frequency: 700 MHz
- Operation Power: 28～40W **(40～57mW/MHz)**

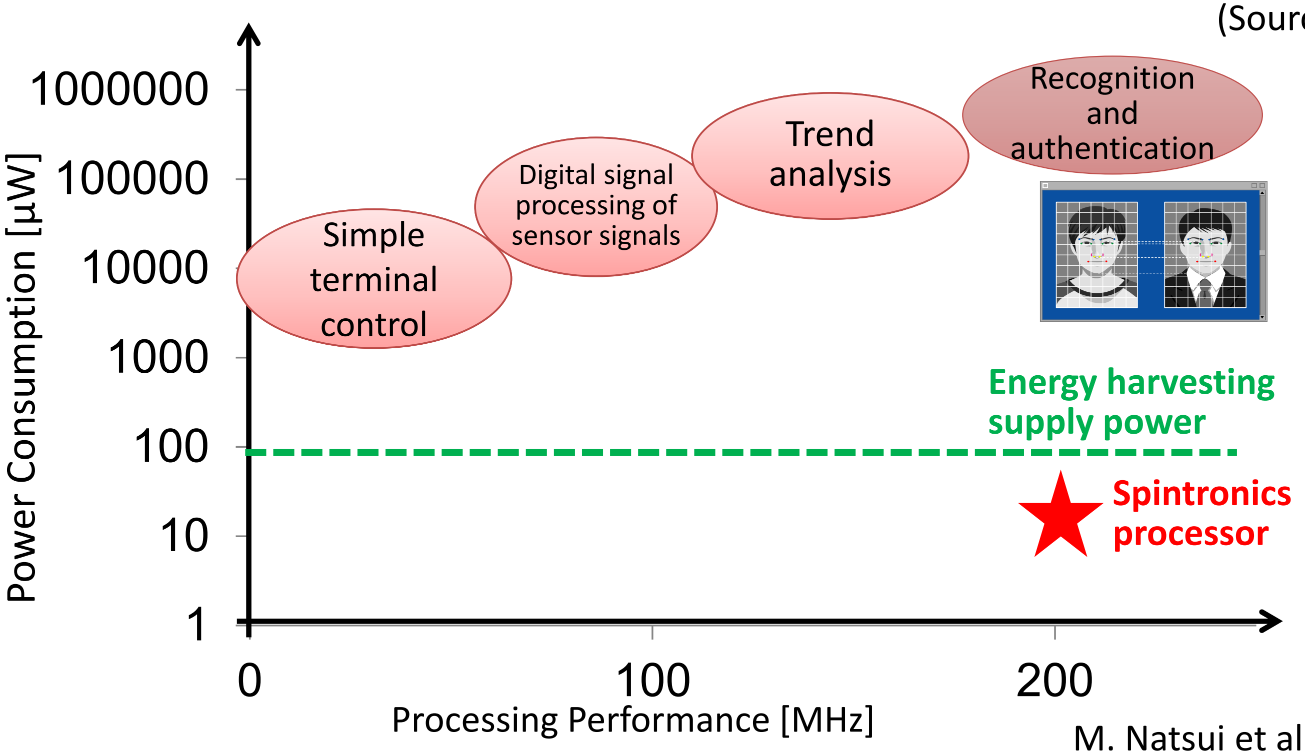
AI chip requirement for autonomous driving

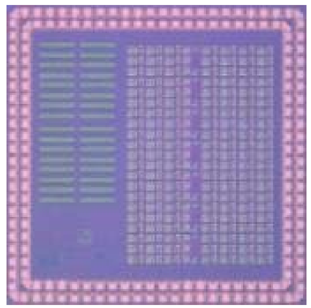


Ultralow energy consumption processor

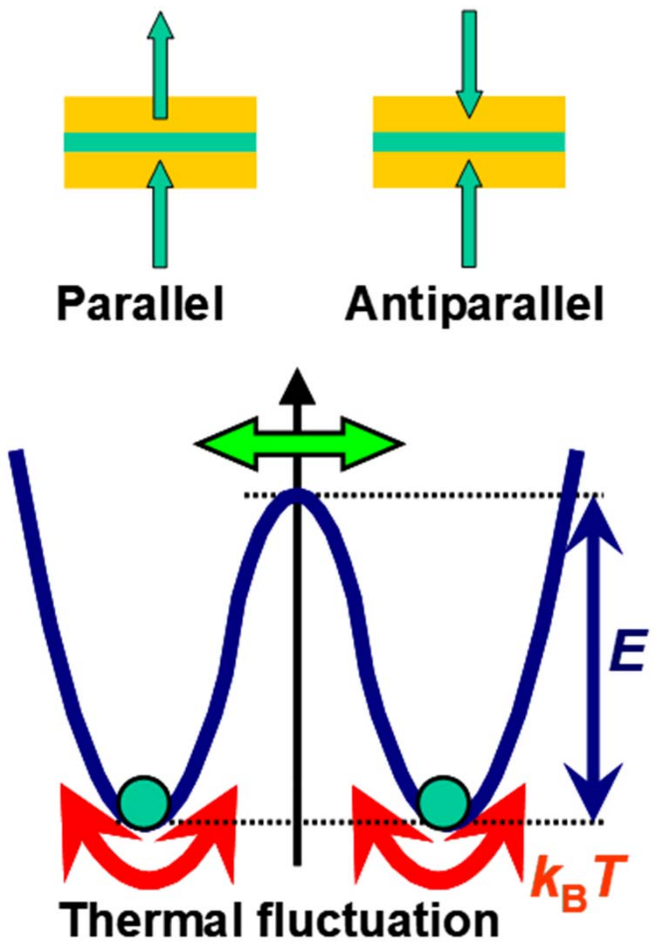
(Source) : Renesas

Nikkei, Feb. 19, 2019

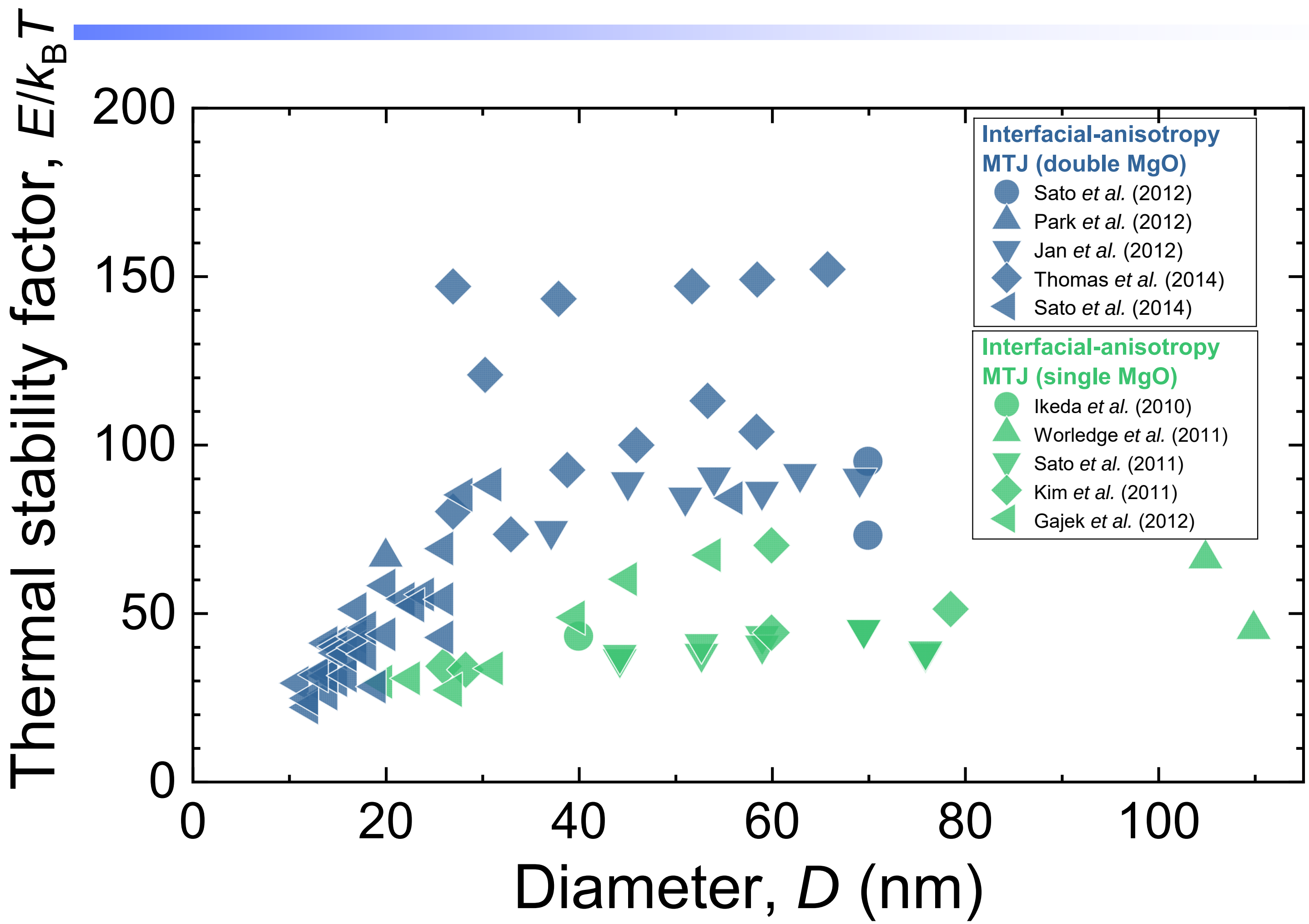




M. Natsui et al., ISSCC 2019.



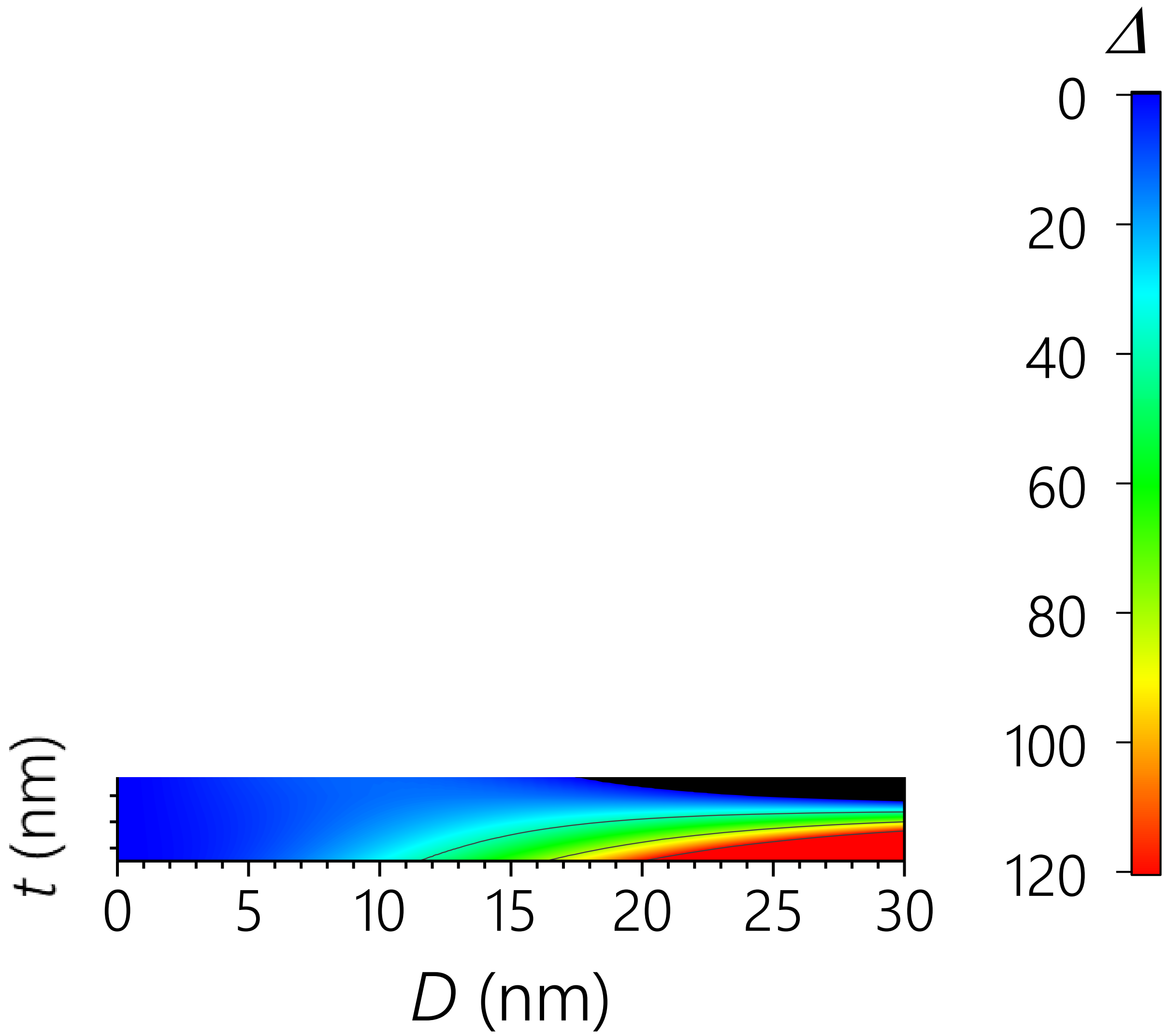
$$E = -\frac{M_S^2}{2\mu_0}V + K_i S$$



After B. Jinnai *et al.*, Appl. Phys. Lett. **116**, 160501 (2020).

Physical Vapor Deposition System (300mm)

http://www.tel.co.jp/news/2014/1201_001.htm

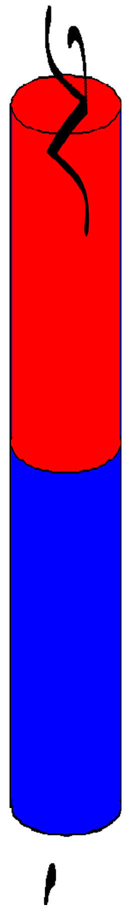


Δ
0
20
40
60
80
100
120
t (nm)
0
5
10
15
20
25
30
D (nm)

Energy barrier E

$$E = N\frac{M_S^2}{2\mu_0}V + K_i S$$

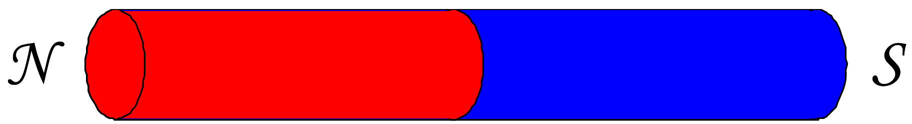
V: volume
S: area



shape anisotropy

interface anisotropy

N: demagnetization factor

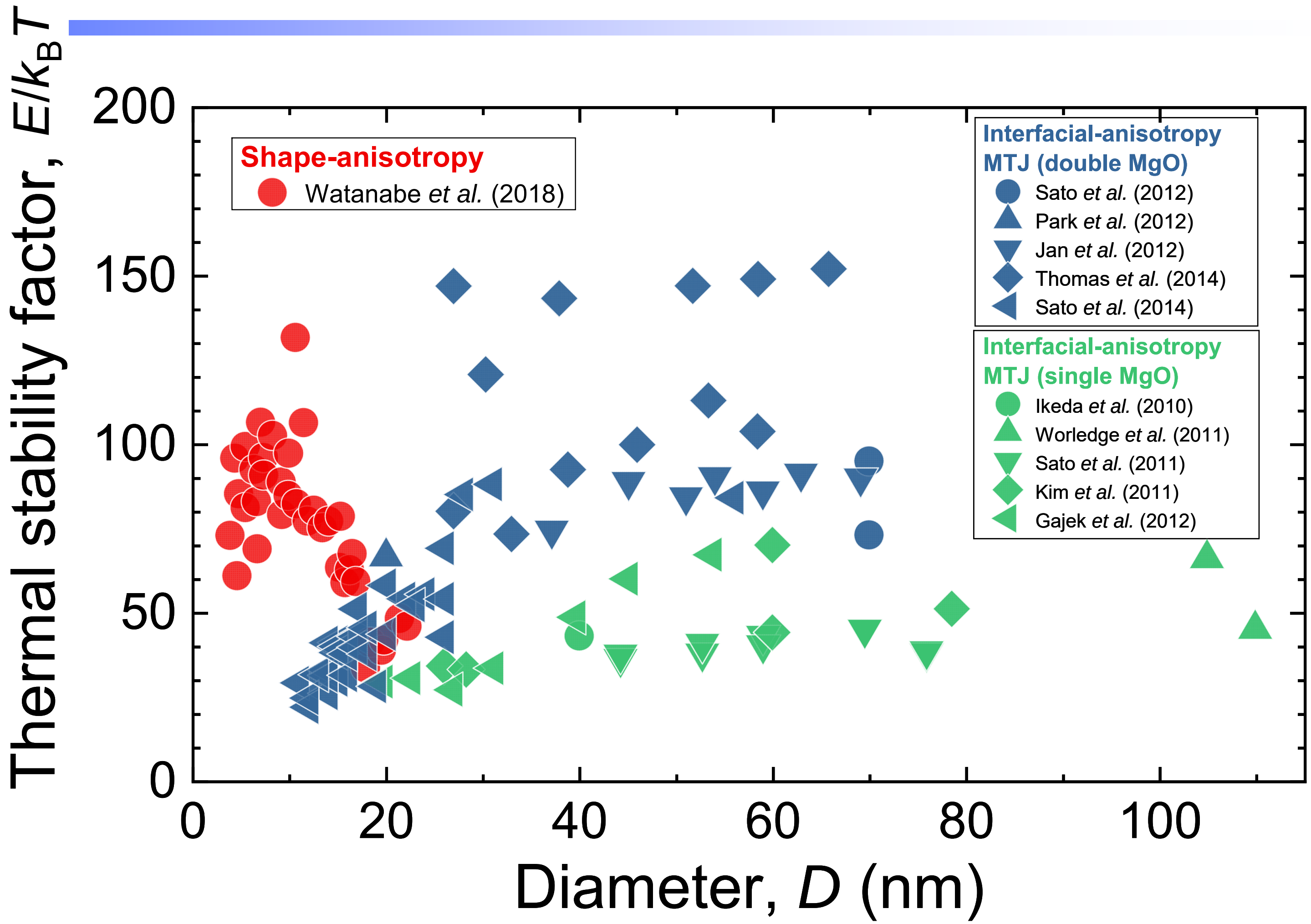


$K_\mathrm{i} > 0$

$N = 1$ (perpendicular)

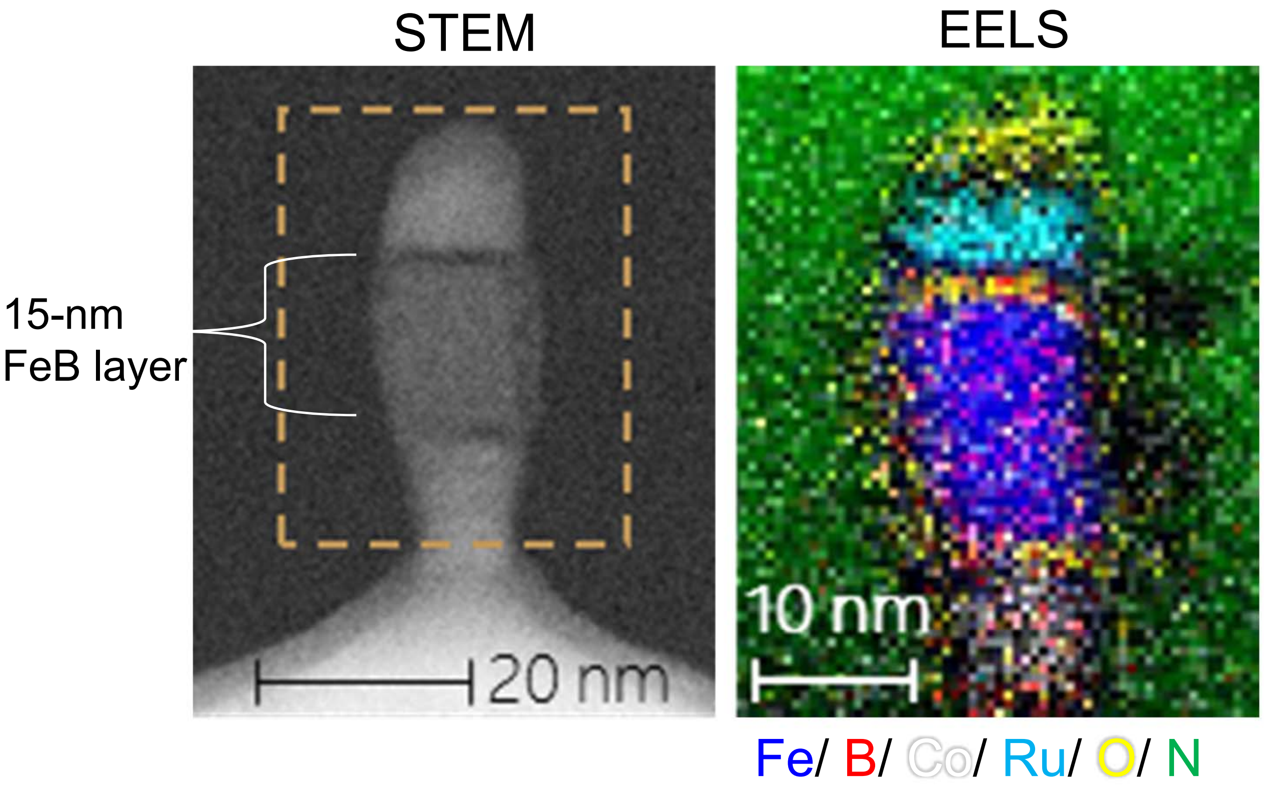
$N = 1$ (in plane)

(perpendicular)

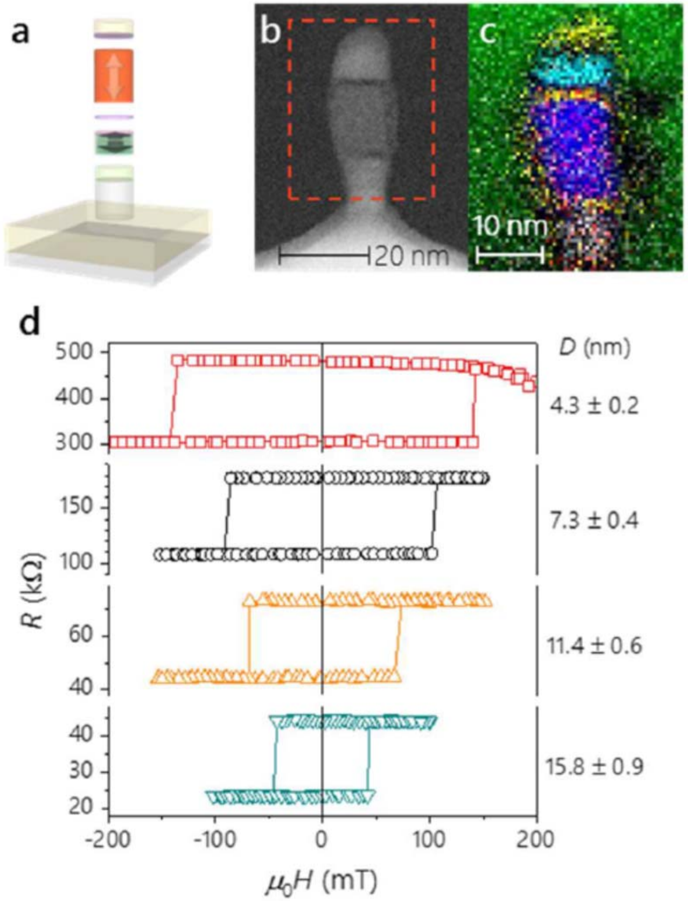


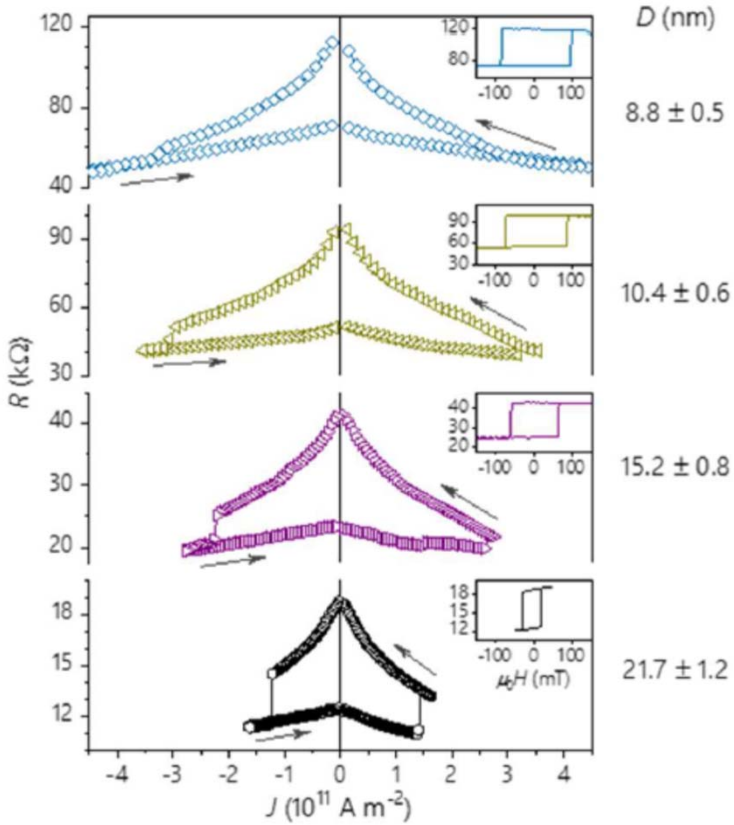
After B. Jinnai *et al.*, Appl. Phys. Lett. **116**, 160501 (2020).

The shape-anisotropy MTJ



K. Watanabe *et al*., Nature Comm. **9**, 663 (2018)

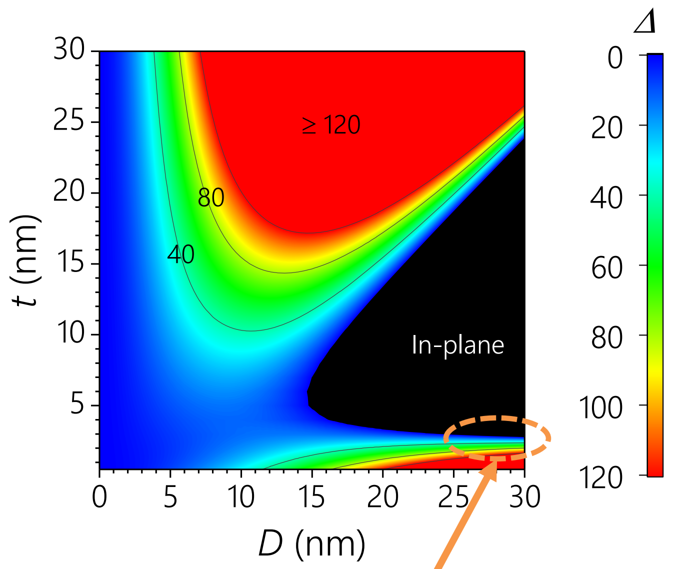




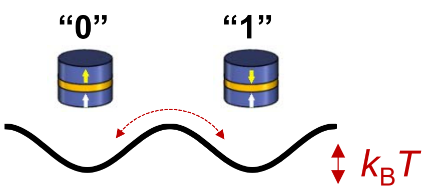
K. Watanabe *et al.*, *Nature Comm.* **9**, 663 (2018)

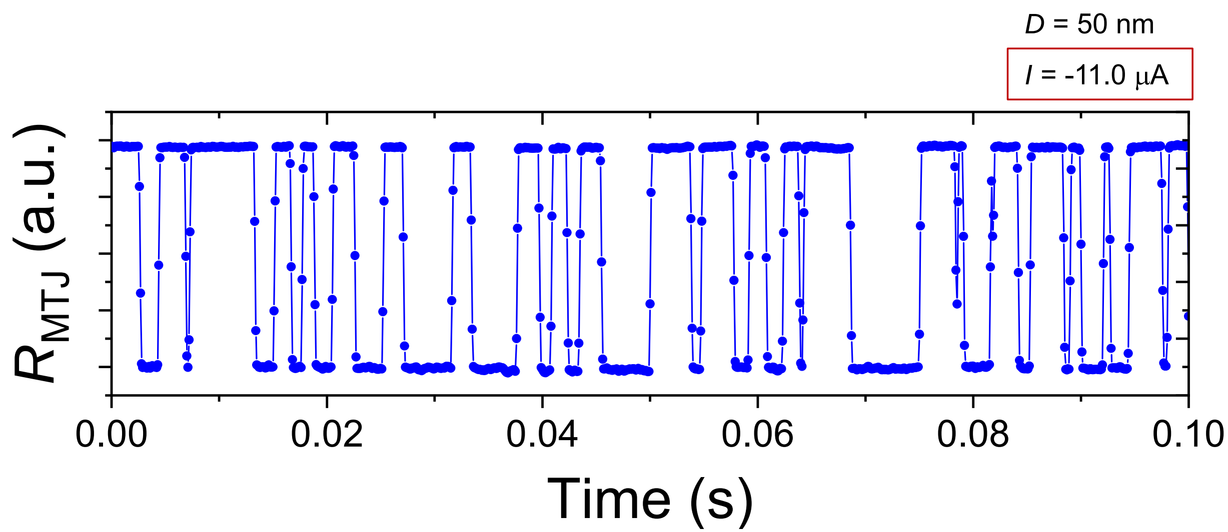
See also, N. Perrissin et al., Nanoscale **10**, 12187 (2018)

Magnetic tunnel junction : $E/k_B T < 20$



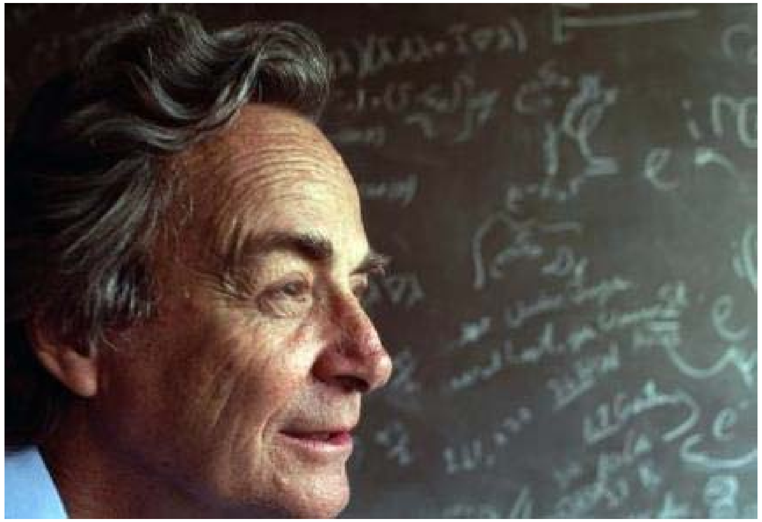
Thermally unstable
(Stochastic)





Lecture by Richard Feynman (1981)

"Simulating Physics with Computers"



https://www.nature.com/articles/d41586-019-02781-4

Physics of Computation Conference
at MIT
on May 6-8, 1981

"If you want to make a simulation of nature, you'd better make it quantum mechanical, …"

⇩

Quantum computing

"…the other way to simulate a probabilistic nature is by a computer which itself is probabilistic, …"

⇩

Probabilistic computing

"Simulating Physics with Computers", International Journal of Theoretical Physics **21**, 467-488 (1982).

Probabilistic computing

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- Boltzmann distribution

$$P(E,T) = \frac{1}{Z}\exp\left[-\frac{E(\Gamma)}{k_\mathrm{B}T}\right]$$

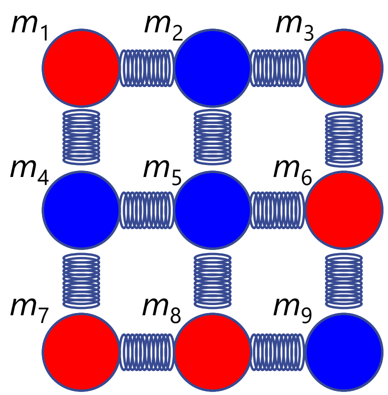
The lowest energy state is most-frequently observed.

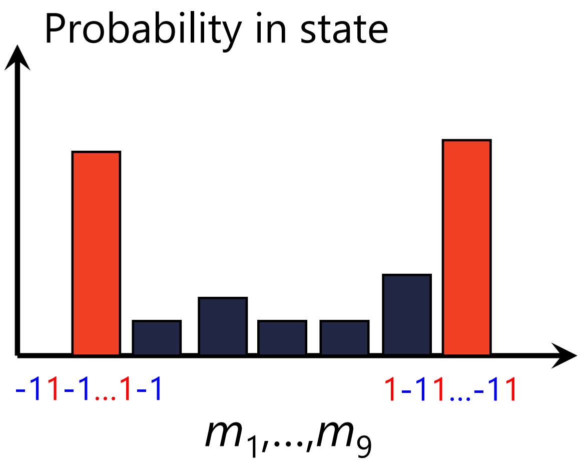
→ Probabilistic computing

Procedure of probabilistic computing

1. Define an **energy (cost function)** for each given problem.
2. Mapping the cost function to a **physical system with probabilistic nature (stochastic neurons)**.
3. Acquiring **statistics**.
4. The most frequent state is the “answer”.

$$E = -\sum J_{ij} m_i m_j$$





What we did …

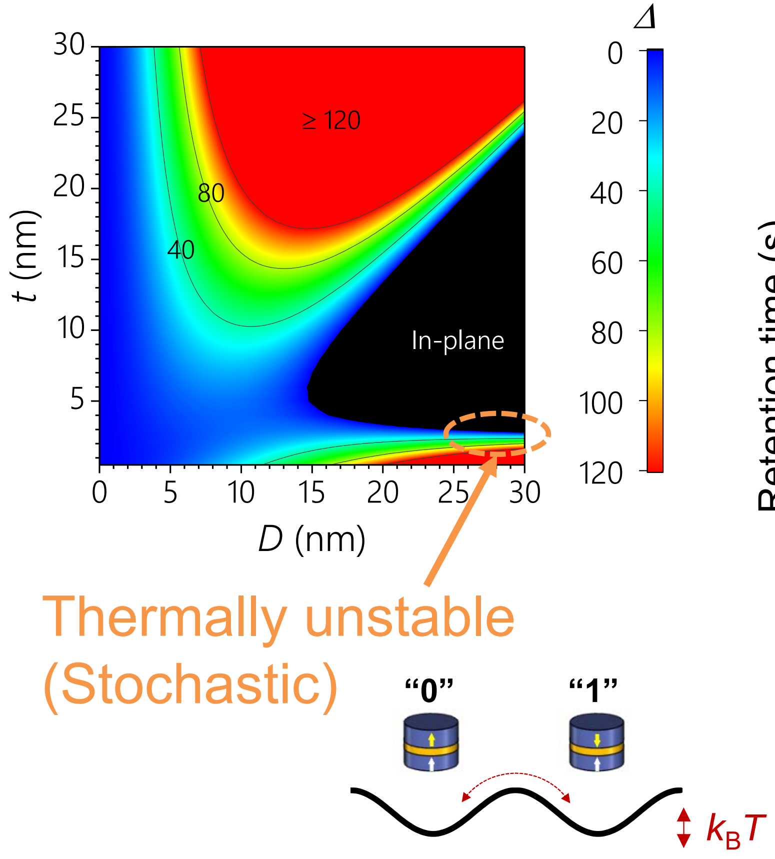
Device → Bit → Circuit → Algorithm

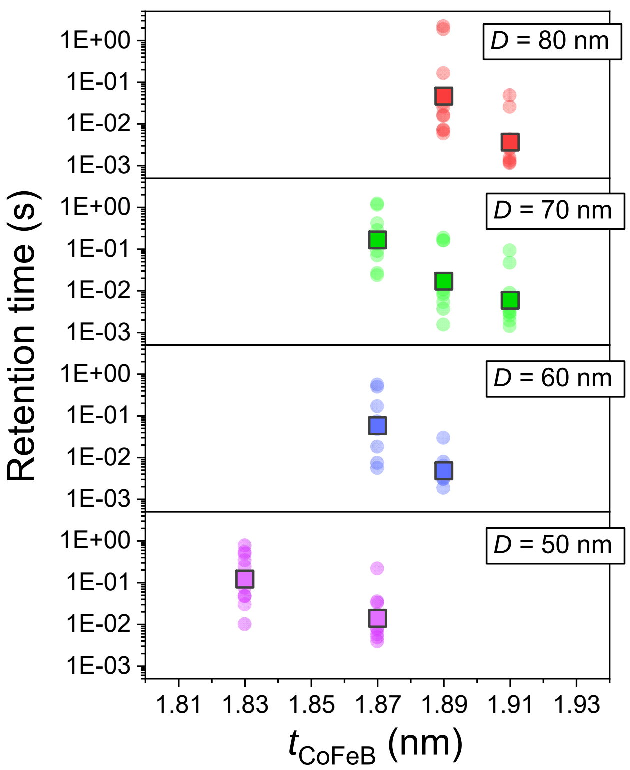
Device	Bit	Circuit	Algorithm
Controllable stochasticity	Sigmoidal response	Connected by synaptic weight logic	Mapping cost function to system

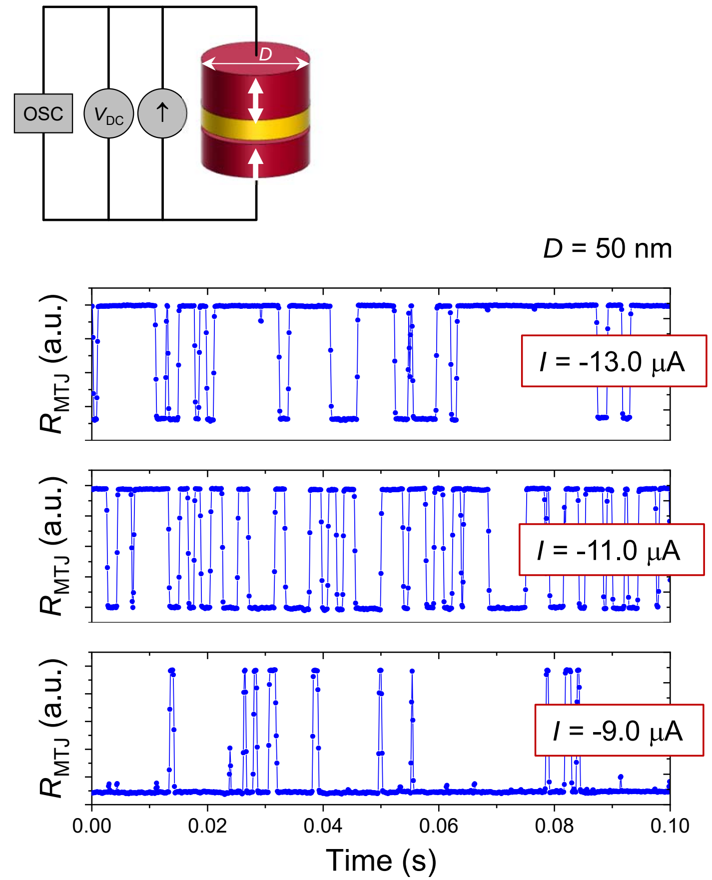
⇨ **Integer factorization**
(illustrative example of optimization)

Stochastic magnetic tunnel junction

Device → Bit → Circuit → Algorithm

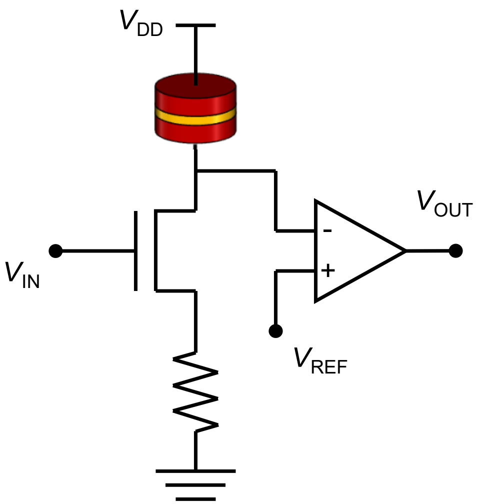


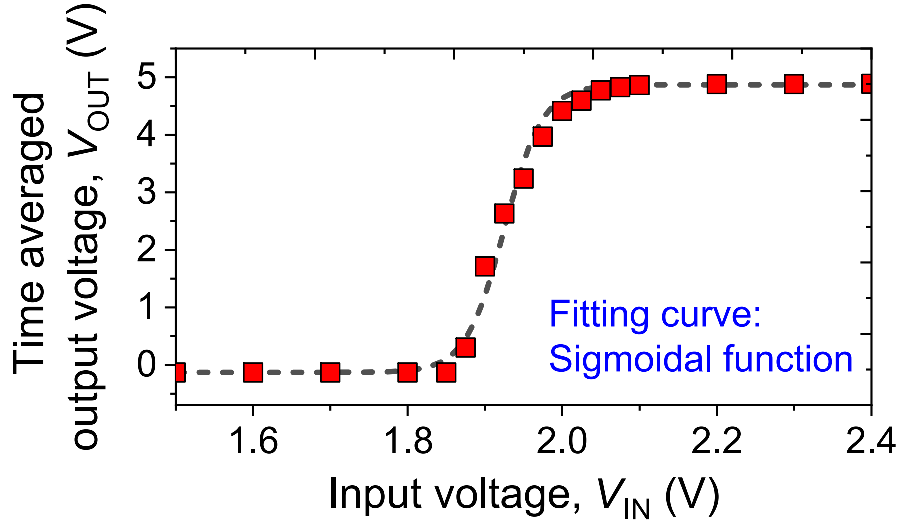


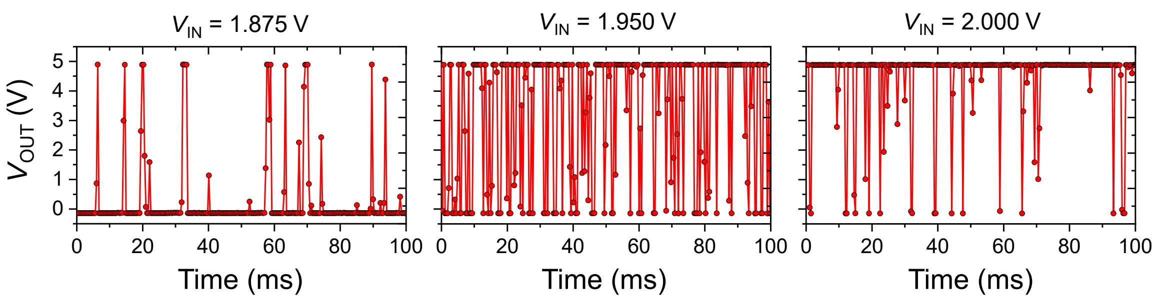


Probabilistic bit (p-bit)

Device | Bit | Circuit | Algorithm



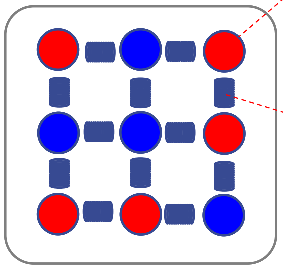


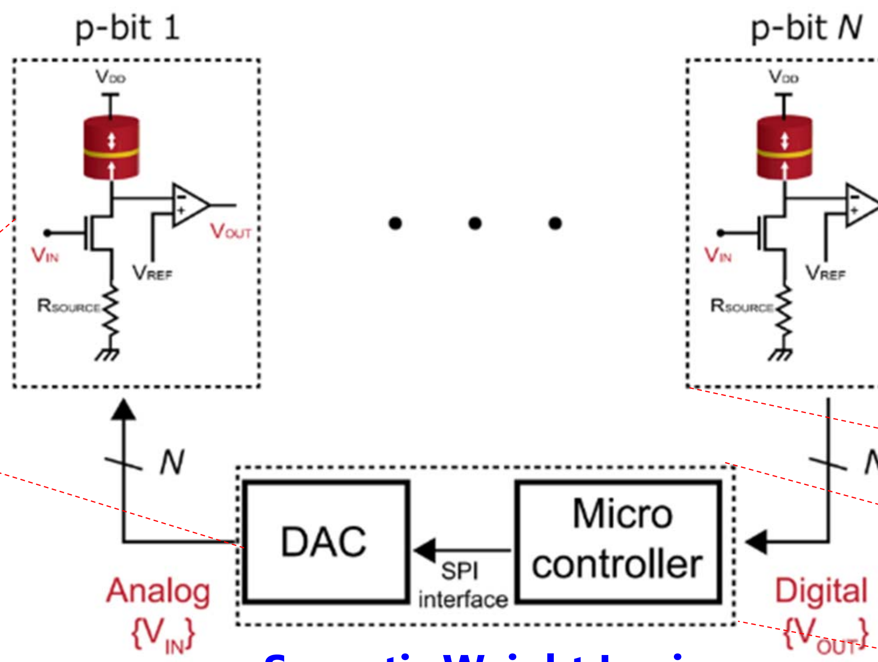


K. Y. Camsari *et al.*, IEEE Elec. Dev. Lett. **38**, 1767 (2017).

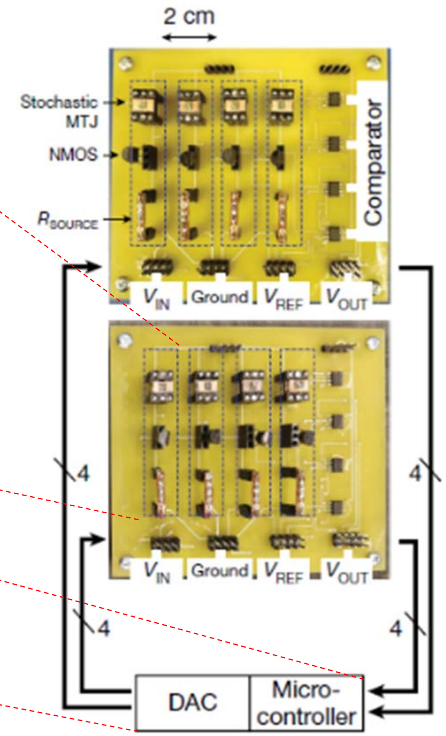
Probabilistic circuit (p-circuit)

Device | Bit | Circuit | Algorithm





Synaptic Weight Logic
(Micro-controller)



Cost function for integer factorization

Device | Bit | Circuit | **Algorithm**

$$E = (XY - F)^2 \qquad \begin{cases} X = 1 + 2x_1 + 4x_2 + 8x_3 + \cdots \\ Y = 1 + 2y_1 + 4y_2 + 8y_3 + \cdots \end{cases}$$

◆ **Example) Factorizing 35 (= *F*) by 4 bits (x_1, x_2, y_1, y_2)**

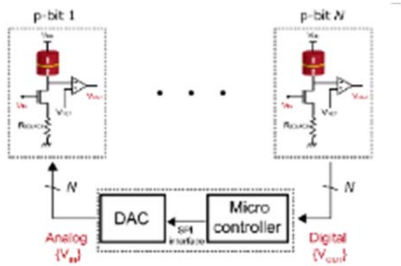
coefficients are rounded off to have one significant digit.

$$E = -0.3x_1 - 0.7x_2 - 0.3y_1 - 0.7y_2 - x_2y_1 - 1.4x_2y_2 - 0.6x_1y_1$$
$$-x_1y_2 + 0.3\underline{x_1y_1y_2} + \underline{x_2y_1y_2} + 0.3\underline{x_1x_2y_1} + \underline{x_1x_2y_2} + 0.7\underline{x_1x_2y_1y_2}$$

3-body interaction

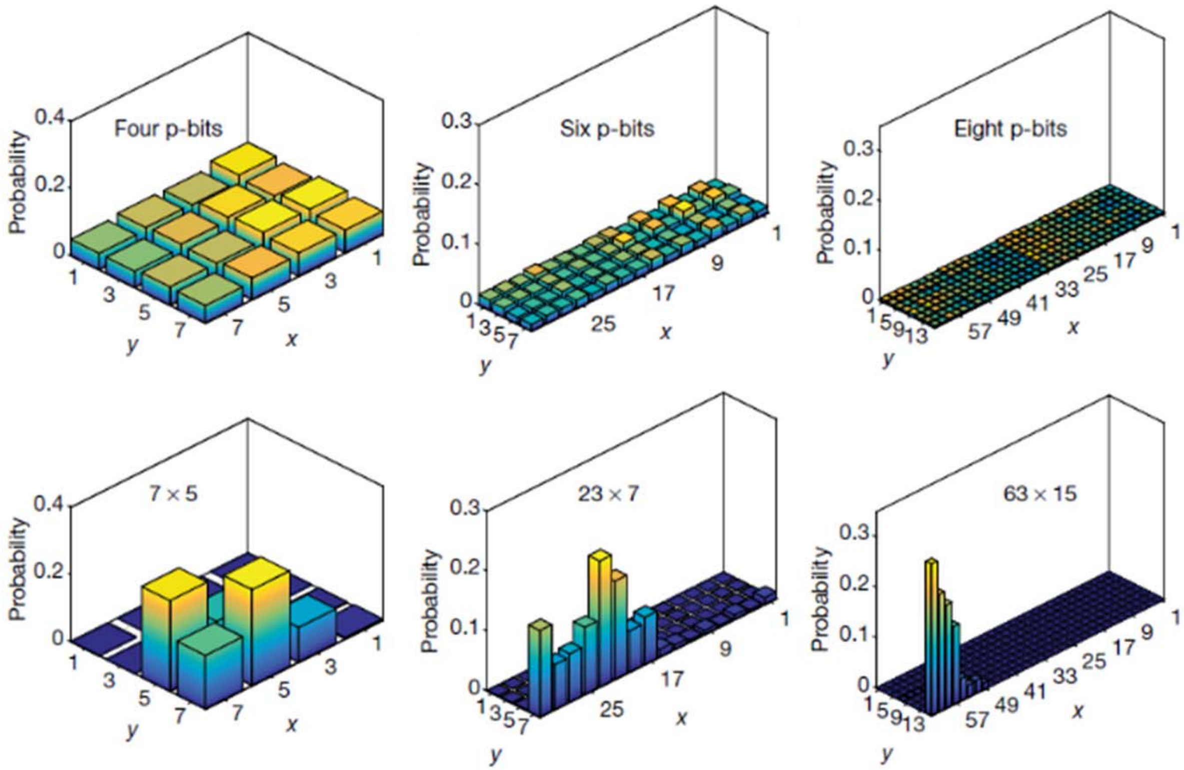
4-body interaction

$$\begin{cases} I_{x1} = -\dfrac{\partial E}{\partial x_1} = 0.3 + 0.6y_1 + 1.0y_2 - 0.3y_1y_2 - 0.3x_2y_1 - 1.0x_2y_2 - 0.7y_1x_2y_2 \\ I_{x2} = -\dfrac{\partial E}{\partial x_2} = 0.7 + 1.0y_1 + 1.4y_2 - 1.0y_1y_2 - 0.3x_1y_1 - 1.0x_1y_2 - 0.7x_1y_1y_2 \\ I_{y1} = -\dfrac{\partial E}{\partial y_1} = 0.3 + 0.6x_1 + 1.0x_2 - 0.3x_1y_2 - 1.0x_2y_2 - 0.3x_1x_2 - 0.7x_1x_2y_2 \\ I_{y2} = -\dfrac{\partial E}{\partial y_2} = 0.7 + 1.0x_1 + 1.4x_2 - 0.3y_1x_1 - 1.0y_1x_2 - 1.0x_1x_2 - 0.7x_1x_2y_1 \end{cases}$$



Results of integer factorization

F = 35 161 945



← Uncorrelated

← Correlated

$X \times Y$ = 7×5 23×7 63×15

W. A. Borders *et al.*, Nature **573**, 390 (2019).

Comparison with quantum annealing machine

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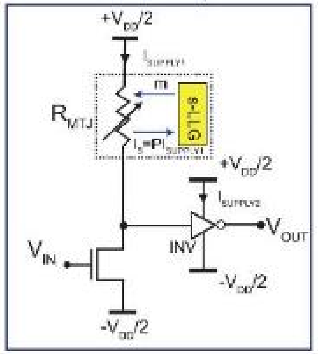
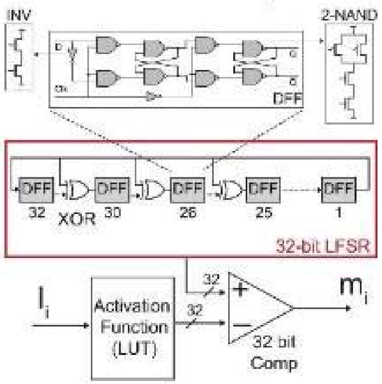
- Room temperature
- Manufacturable at the Mb-Gb level (STT-MRAM)
- Can implement many-body interactions easily
- No quantum supremacy

Comparison with CMOS-based simulated annealing

- MTJ-based p-bit



- Digital CMOS-based p-bit



LFSR: Linear-feedback shift register
LUT: Look-up table